

CRYSTAL CLEAR TECHNOLOGY

Product Specification

T350T14X00

(REVISION 2)

Crystal Clear Technology Sdn. Bhd.

16 Jalan TP5, Taman Perindustrian Sime UEP,

47600 Subang Jaya, Selangor DE

Tel: +603-80247099

Website: www.cct.com.my



2.0 Records of Revision

Rev	Date	Item	Page	Comment	Originator	Checked By
1.0	19.12.16			Initial Release	SCChong	Azhar
2.0	14.03.17			Add new CTP version	Azhar	Azhar



3.0 General Specification

T350T14X00 is 3.5" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs control circuit and LED backlight. This display area contains 320 x 240 pixels and can display up to 262k colors. This product compliant with RoHS environmental requirement.

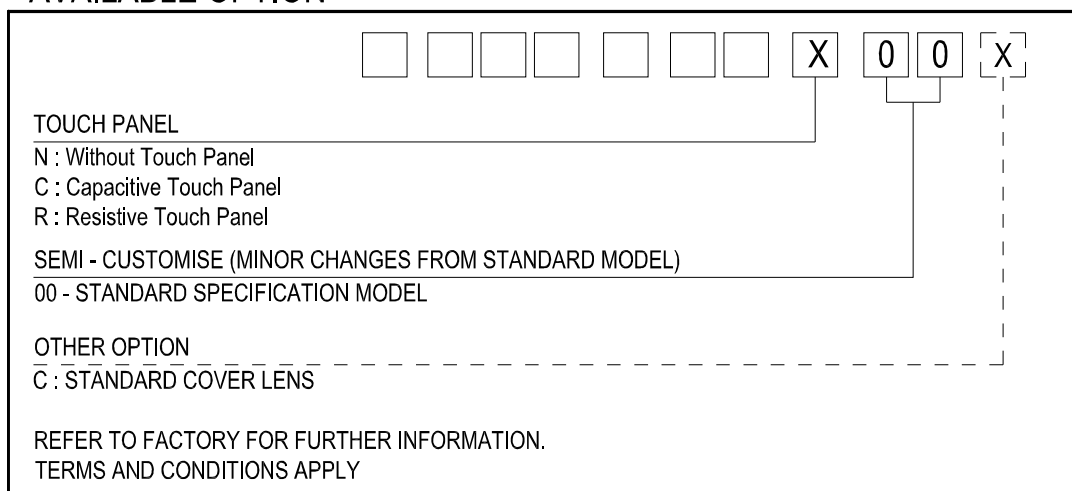
Item	Contents	Unit	Note
LCD Type	3.5" TFT	-	
Display color	262k		1
Viewing Direction (Optimum View)	12	O'Clock	
Module size	76.87(W) x 63.90(H) x 3.27(T)	mm	2
Active Area(W×H)	70.08(H) x 52.56(V)	mm	
Number of Dots	320×RGB×240	dots	
Controller	SSD2119 or equivalent	-	
Backlight	6 White LEDs	pcs	
Brightness	300	cd/m2	
Interface Mode	1. 8/9/16/18-bit MCU 2. 3 SPI / 4 SPI 3. 6/16/18-bit RGB	-	
Data Transfer	RGB	-	

Note1: Color tone is slightly changed by temperature and driving voltage.

Note2: FPC or wire are not included.

Note3: Brightness on LCD surface. Module with CTP or RTP, brightness will be about 20% (max) lower on the touch panel surface.

AVAILABLE OPTION





4.0 Absolute Maximum Ratings

4.1 Electrical Absolute Maximum ratings (V_{ss} = 0V, Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDDIO	-0.3	4.0	V	1, 2
Input Voltage	VCI	VSS-0.3	5.0	V	
Current of LED	ILED	0	25	mA/led	

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged.
2. V_{CC} > V_{SS} must be maintained.
3. Please be sure users are grounded when handing LCD Module.

4.2 Environmental Absolute Maximum Ratings

Item	Storage		Operating		Note
	MIN.	MAX.	MIN.	MAX.	
Ambient Temperature	-30°C	80°C	-20°C	70°C	1,2
Humidity	-	-	-	-	3

1. The response time will become lower when operated at low temperature.
2. Background color changes slightly depending on ambient temperature. The phenomenon is reversible.
3. Ta ≤ 40°C and 85%RH MAX.
(Ta > 40°C. Absolute humidity must be lower than the humidity of 85%RH at 40°C)



5.0 Electrical Characteristics and Instruction Code

5.1 Electrical Characteristics (V_{SS} = 0V, T_a = 25°C)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ	Max.		
Power Voltage	VDDIO	1.8	-	3.6	V	
Input Voltage	VCI	2.5	-	3.6	V	
Gate ON Voltage	VGH	10	-	16	V	
Gate OFF Voltage	VGL	-16	-	-9	V	
Vcom High Voltage	VcomH	2.5	-	5	V	
Vcom low Voltage	VcomL	-2.5	-	0	V	
Logic High Input Voltage	VIH	0.8VDDIO	-	VDDIO	V	
Logic Low Input Voltage	VIL	0	-	0.2VDDIO	V	
Logic High Output Voltage	VOH	0.9VDDIO	-	VDDIO	V	
Logic Low Output Voltage	VOL	0	-	0.1VDDIO	V	
Supply Current	IDD	TBD	TBD	TBD	mA	

Note:

1. VGH – A positive power output pin for gate driver
2. VGL – A negative power output pin for gate driver
3. VGH and VGL booster ratio can set by the register

5.2 LED Backlight Specification (V_{SS} = 0V, T_a = 25°C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage	V _{LED}	-	17.4	-	20.4	V	1
Supply Current	I _f	-	-	20	-	mA	2
Lifetime			20000	-	-	Cd/m ²	3

Note:

1. V_{LED} = V_{LED} (+) - V_{LED} (-).
2. It is recommended that customer supply constant current to prolong the led lifetime and optimum led performance
3. Definition of Lifetime: Luminance < 50% of initial Luminance
(Test condition: T_a = 25°C, Constant current supply (typical Value))

**5.3 Interface Signal**

Pin No.	Symbol	Function
1 – 2	VLED-	LED back light(Cathode)
3 - 4	VLED+	LED back light(Anode)
5 - 7	NC	No connect
8	RESET	System reset - An active low pulse at this pin will reset the IC. Connect to VDDIO in normal operation.
9	CS	Chip select for 6800/8080 parallel interface and Serial mode interface.
10	SCL	Serial clock input. If not in use, please connect to VSS.
11	SDA	Data input pin in serial interface. If not in use, please connect to VSS.
12	SDO	Data output pin in serial interface. If not in use, please left open.
13	WSYNC	Ram write synchronization output. If not in use, please left open.
14 - 19	D0 – D5	Data bus. Unused pins should connect to VSS. Please refer to Interface Mapping for definition.
20 - 21	NC	No connect
22 - 27	D6 – D11	Data bus. Unused pins should connect to VSS. Please refer to Interface Mapping for definition.
28 - 29	NC	No connect
30 - 35	D12 – D17	Data bus. Unused pins should connect to VSS. Please refer to Interface Mapping for definition.
36	HSYNC	Line synchronous input. If not in use, please connect to VSS.
37	VSYNC	Frame/Ram write synchronous input. If not in use, please connect to VSS.
38	DOTCLK	Dot-clock signal and oscillator source. If not in use, please connect to VSS.
39	VSS	Ground
40	VDDIO	Power supply
41 - 42	VDD	Power supply
43 - 44	NC	No connect
45	RS	Data or Command: 1. Parallel Interface 2. Serial Interface If not in use, please connect to VDDIO or VSS.
46	RD	1. 6800-system – Enable signal 2. 8080-system – Read strobe signal 3. Serial mode – Connect to VDDIO or VSS
47	RW	1. 6800-system – Read/Write signal



		2. 8080-system – Write strobe signal 3. Serial mode – Connect to VDDIO or VSS
48	PS3	Interface selection pin: More detail, please refer to Table 1
49	PS2	
50	PS1	
51	PS0	
52	DEN	Display enable pin. If not in use, please connect to VSS.
53 - 54	VSS	Ground

Table 1: Interface selection

PS3	PS2	PS1	PS0	Interface Mode	Data bus input
0	0	0	0	16-bit 6800 parallel interface	D[17:10], D[8:1]
0	0	0	1	8-bit 6800 parallel interface	D[17:10]
0	0	1	0	16-bit 8080 parallel interface	D[17:10], D[8:1]
0	0	1	1	8-bit 8080 parallel interface	D[17:10]
0	1	0	0	9-bit generic D[9:16] (262k colour) + 3-wire SPI If 65K color, D12 shorts to D17 internally	
0	1	0	1	16-bit generic (262k colour) + 3-wire SPI	
0	1	1	0	18-bit generic (262k colour) + 3-wire SPI	
0	1	1	1	6-bit generic D[8:3] (262k colour) + 3-wire SPI	
1	0	0	0	18-bits 6800 parallel interface	D[17:0]
1	0	0	1	9-bits 6800 parallel interface	D[17:9]
1	0	1	0	18-bit 8080 parallel interface	D[17:0]
1	0	1	1	9-bit 8080 parallel interface	D[17:9]
1	1	1	0	3-wire SPI	
1	1	1	1	4-wire SPI	



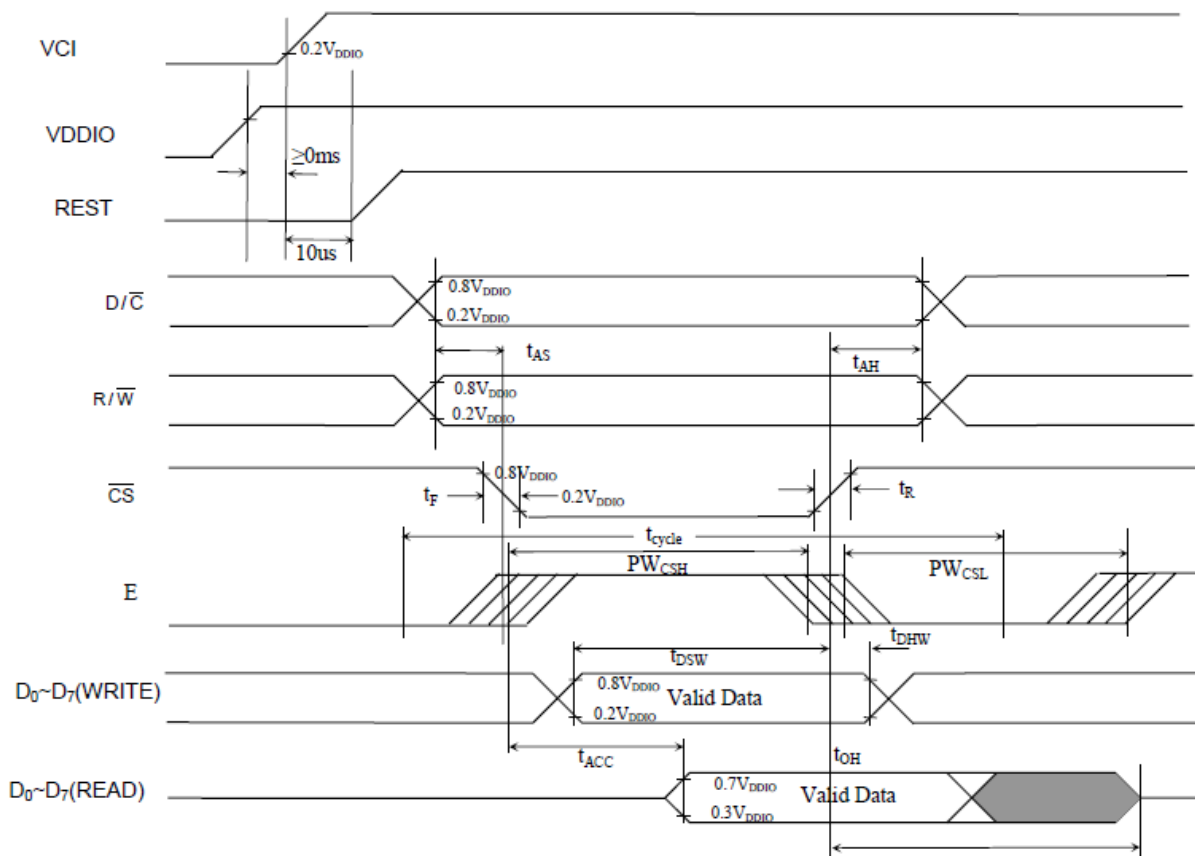
6.0 AC characteristics

6.1 Parallel 6800 Timing Characteristics

($T_A = -40$ to 85°C , $V_{DDIO} = 1.4\text{V}$ to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on $V_{OL}/V_{OH} = 0.3 \cdot V_{DDIO}/0.7 \cdot V_{DDIO}$)	450	-	-	ns
t_{AS}	Address Setup Time (R/ \bar{W})	0	-	-	ns
t_{AH}	Address Hold Time (R/ \bar{W})	0	-	-	ns
t_{DSW}	Data Setup Time (D0-D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0-D7, WRITE)	5	-	-	ns
t_{ACC}	Data Access Time (D0-D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0-D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled





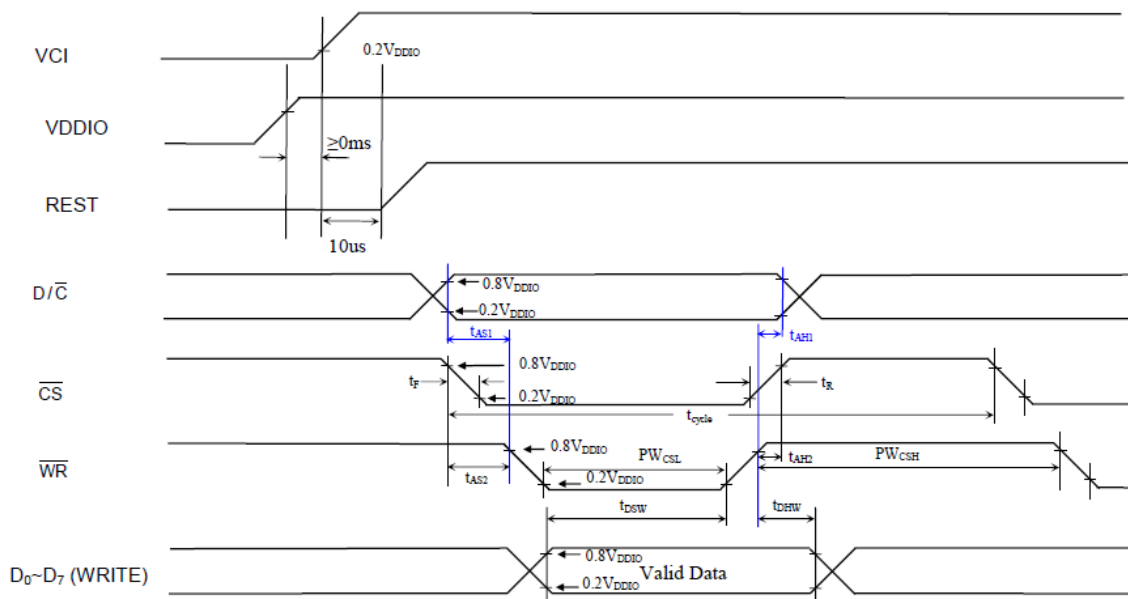
6.2 Parallel 8080 Timing Characteristics

($T_A = -40$ to 85°C , $V_{DDIO} = 1.4\text{V}$ to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on $V_{OL}/V_{OH} = 0.3 \cdot V_{DDIO}/0.7 \cdot V_{DDIO}$)	450	-	-	ns
t_{AS1}	Address Setup Time between (R/\bar{W}) and D/\bar{C}	0	-	-	ns
t_{AH1}	Address Hold Time between (R/\bar{W}) and D/\bar{C}	0	-	-	ns
t_{AS2}	Address Setup Time between (R/\bar{W}) and \bar{CS}	0	-	-	ns
t_{AH2}	Address Hold Time between (R/\bar{W}) and \bar{CS}	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE)	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

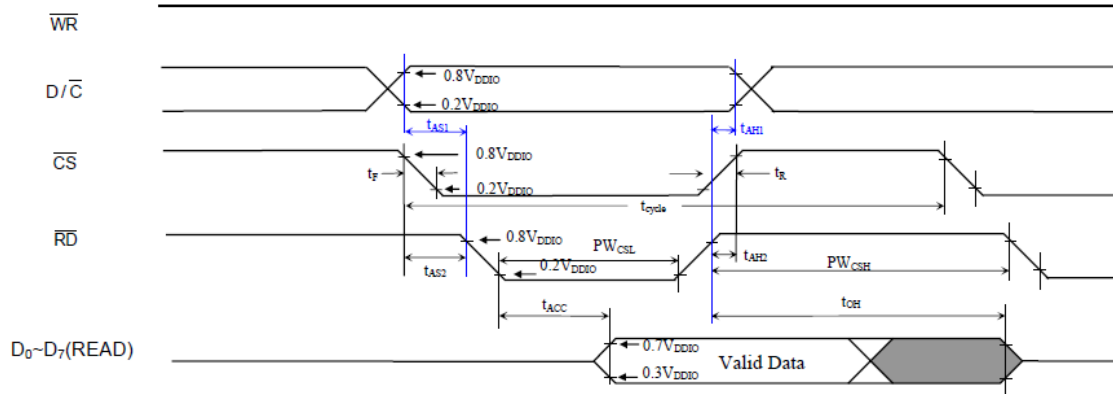
Note: CS can be pulled low during the write cycle, only R/\bar{W} is needed to be toggled

Write Cycle



Remark: It's highly recommended that \bar{RD} remains high for the whole write cycle

Read Cycle

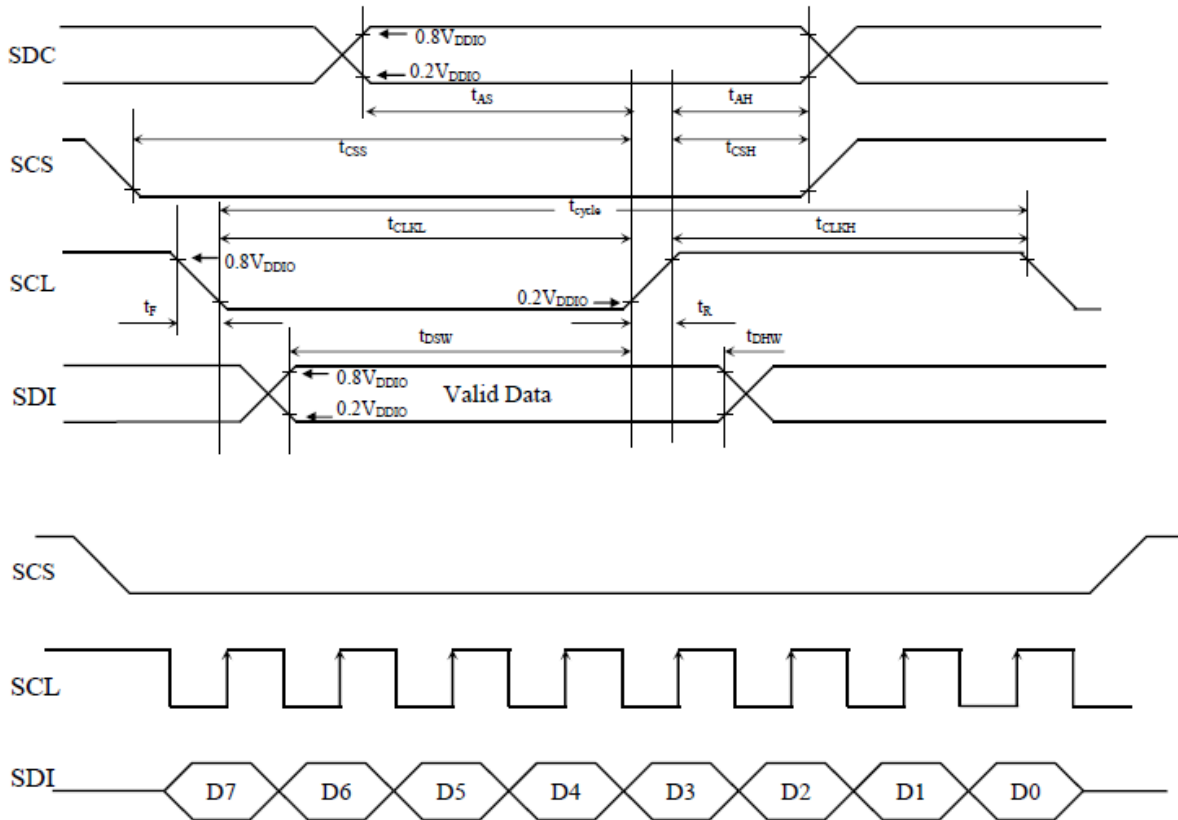




6.3 Serial Timing Characteristics

($T_A = -40$ to 85°C , $V_{DDIO} = 1.4\text{V}$ to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	77	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	4	-	-	ns
t_{AH}	Register select Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	5	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	38	-	-	ns
t_{CLKH}	Clock High Time	38	-	-	ns
t_{R}	Rise time	-	-	4	ns
t_{F}	Fall time	-	-	4	ns



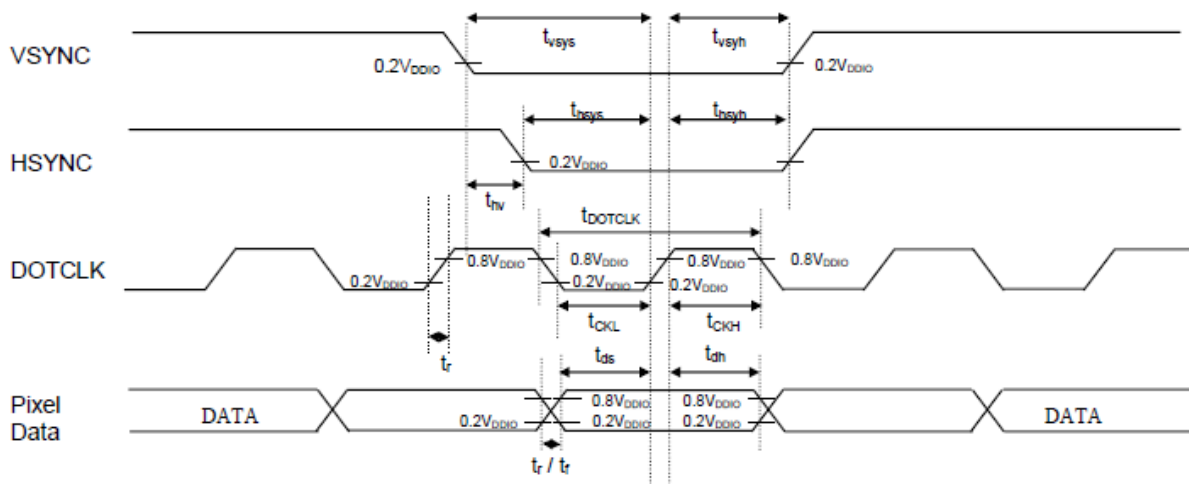


6.4 RGB Timing Characteristics

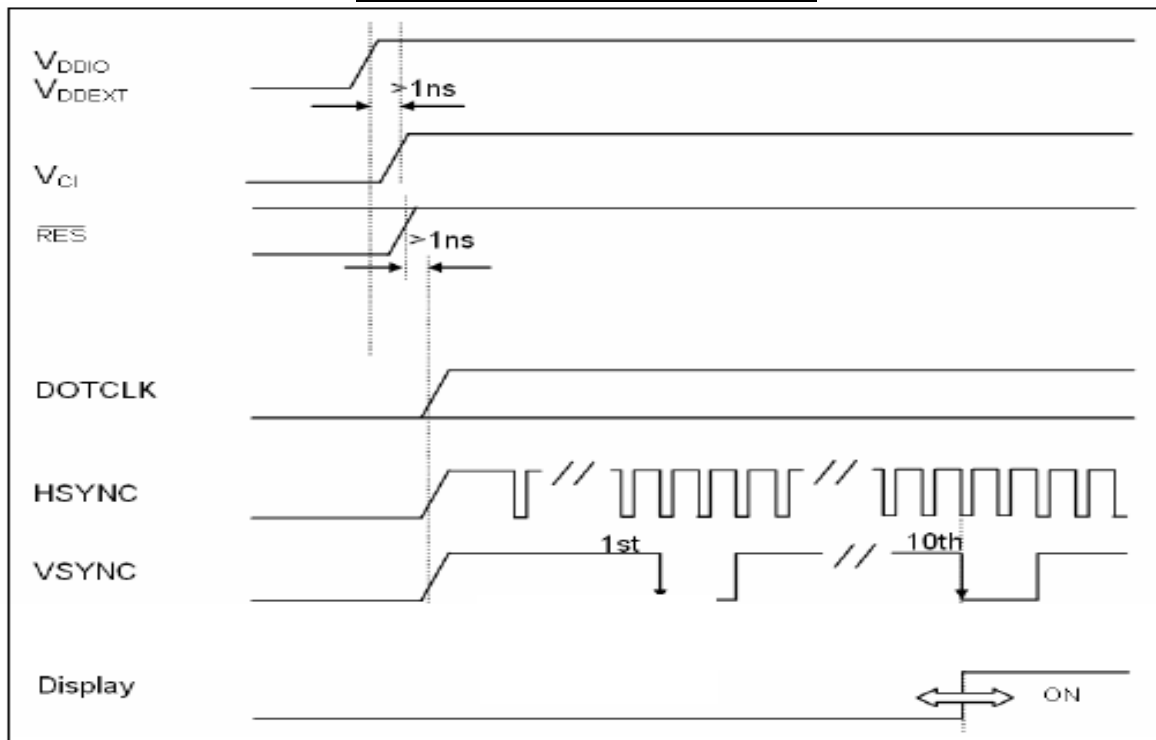
($T_A = -40$ to 85°C , $V_{DDIO} = 1.4\text{V}$ to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
f_{DOTCLK}	DOTCLK Frequency (70Hz frame rate)	1	5.5	8.2	MHz
t_{DOTCLK}	DOTCLK Period	122	182	1000	ns
t_{VSYN}	Vertical Sync Setup Time	20	-	-	ns
t_{VSYH}	Vertical Sync Hold Time	20	-	-	ns
t_{HSYN}	Horizontal Sync Setup Time	20	-	-	ns
t_{HSYH}	Horizontal Sync Hold Time	20	-	-	ns
t_{HV}	Phase difference of Sync Signal Falling Edge	0	-	320	t_{DOTCLK}
t_{CLKL}	DOTCLK Low Period	61	-	-	ns
t_{CKH}	DOTCLK High Period	61	-	-	ns
t_{DS}	Data Setup Time	25	-	-	ns
t_{DH}	Data hold Time	25	-	-	ns

Note: External clock source must be provided to DOTCLK pin of SSD2119. The driver will not operate in absence of the clocking signal.

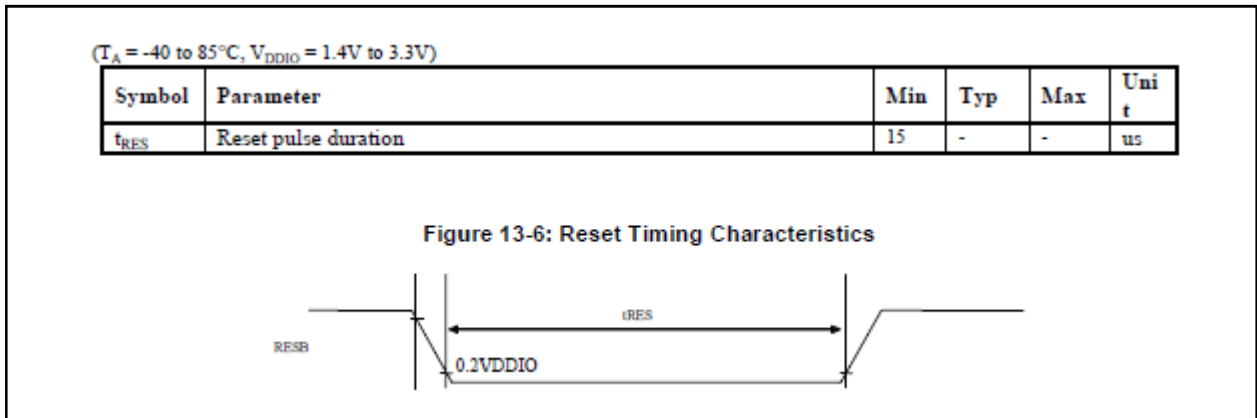


Power up Sequence for RGB Mode





6.5 Reset Timing



6.6 Interface Mapping

6.6.1 Mapping for Writing Instruction

Interface	Cycle	Hardware pins																	
		D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18 bits		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	x	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	x
16 bits		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8		IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
9 bits	1 st	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	x									
	2 nd	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	x									
8 bits	1 st	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8										
	2 nd	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0										

Remark : x Don't care bits
 Not connected pins

6.6.2 Mapping for Writing Pixel Data

Interface	Color mode	Cycle	Hardware pins																		
			D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
18 bits	262k		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	
16 bits	262k	1 st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x		
		2 nd	B5	B4	B3	B2	B1	B0	x	x		R5	R4	R3	R2	R1	R0	x	x		
		3 rd	G5	G4	G3	G2	G1	G0	x	x		B5	B4	B3	B2	B1	B0	x	x		
		1 st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x		
		2 nd	x	x	x	x	x	x	x	x		B5	B4	B3	B2	B1	B0	x	x		
		2 nd	B5	B4	B3	B2	B1	B0	x	x		x	x	x	x	x	x	x	x	x	
9 bits	262k	1 st	R4	R3	R2	R1	R0	G5	G4	G3		G2	G1	G0	B4	B3	B2	B1	B0		
		2 nd	R5	R4	R3	R2	R1	R0	G5	G4	G3										
8 bits	262k	1 st	R5	R4	R3	R2	R1	R0	x	x											
		2 nd	G5	G4	G3	G2	G1	G0	x	x											
		3 rd	B5	B4	B3	B2	B1	B0	x	x											
		1 st	R4	R3	R2	R1	R0	G5	G4	G3											
		2 nd	G2	G1	G0	B4	B3	B2	B1	B0											
		2 nd	G2	G1	G0	B4	B3	B2	B1	B0											

Remark : x Don't care bits
 Not connected pins

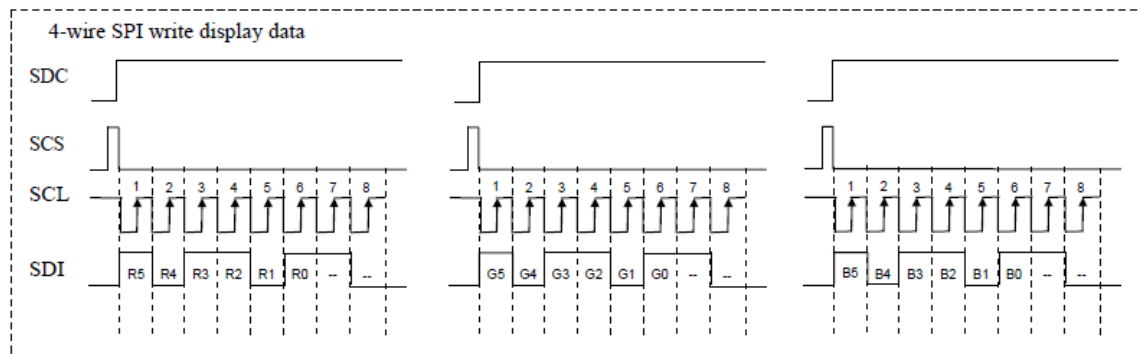
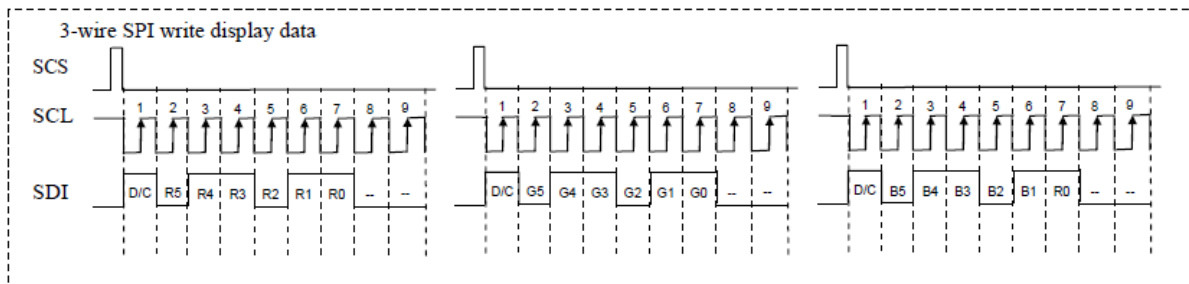


6.6.3 Mapping for Writing Pixel Data in Generic mode

Interface	Color mode	Cycle	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18-bit RGB PS=[0110]	262k	-	RR5	RR4	RR3	RR2	RR1	RR0	GG5	GG4	GG3	GG2	GG1	GG0	BB5	BB4	BB3	BB2	BB1	BB0
18-bit RGB PS=[0110]	65k	-	RR4	RR3	RR2	RR1	RR0	RR4	GG5	GG4	GG3	GG2	GG1	GG0	BB4	BB3	BB2	BB1	BB0	BB4
16-bit RGB PS=[0101]	65k	-	RR4	RR3	RR2	RR1	RR0	GG5	GG4	GG3		GG2	GG1	GG0	BB4	BB3	BB2	BB1	BB0	
9-bit RGB	262k	1 st	RR5	RR4	RR3	RR2	RR1	RR0	GG5	GG4	GG3									
		2 nd	BB5	BB4	BB3	BB2	BB1	BB0	GG2	GG1	GG0									
6-bit RGB	262k	1 st	RR5	RR4	RR3	RR2	RR1	RR0												
		2 nd	GG5	GG4	GG3	GG2	GG1	GG0												
		3 rd	BB5	BB4	BB3	BB2	BB1	BB0												

Remark: Not Connected pins

6.6.4 Mapping for Writing Pixel Data in SPI Mode





6.7 Command Table

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
R	Index	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
R00h	Oscillation Start (0000h)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R01h	Driver output control (3AEFh)	0	1	0	RL	REV	GD	BGR	SM	TB	0	MUX7	MUX5	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0	
R02h	LCD drive AC control (0000h)	0	1	0	0	0	FLD	ENW3	B/C	EOR	W3MD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0	
R03h	Power control (1) All GAM45[2:0] setting 8 color (5A64h)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0	
R07h	Display control (0000h)	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	DD	
R0Bh	Frame cycle control (5308h)	0	1	NO1	NO0	SOT1	SOT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0	
R0Ch	Power control (2) (0004h)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0	
R0Dh	Power control (3) (0000h)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0	
R0Eh	Power control (4) (0000h)	0	1	0	0	VCOM3	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0	
R0Fh	Gate scan start position (0000h)	0	1	0	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R10h	Sleep mode (0001h)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP
R11h	Entry mode (6230h)	0	1	VS mode	DFM1	DFM0	0	Denmode	WMode	Nosync	DMode	TY1	TY0	ID1	ID0	AM	0	0	0	
R12h	Sleep mode (0D99h)	0	1	0	0	OSLP	0	1	1	0	1	1	0	0	1	1	0	0	0	1
R15h	Entry mode (B010h)	0	1	1	0	1	1	0	0	0	0	0	0	0	1	INVDOT	INVDEN	INVHS	INVVS	
R16h	Horizontal Porch (001Dh)	0	1	0	0	0	0	0	0	0	0	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	
R17h	Vertical Porch (0003h)	0	1	VFP7	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	noTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	
R20h	Uniformity (B0EBh)	0	1	1	0	1	1	0	0	0	0	1	1	ENSVIN	0	1	0	1	1	
R22h	RAM data write RAM data read	0 1	1 1	Data[17:0] mapping depends on the interface setting																
R25h	Frame Frequency (8000h)	0	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0	
R26h	Analogue Setting (3800h)	0	1	0	RW_T	VCB	RLTM	ENN	0	0	0	0	0	0	0	0	0	0	0	
R28h	VCOM OTP (000Ah)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	
R29h	VCOM OTP (80C0h)	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00	
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20	
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40	
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00	
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00	
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20	
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40	
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00	
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00	
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00	
R41h	Vertical scroll control (1) (0000h)	0	1	0	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10



Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R42h	Vertical scroll control (2) (0000h)	0	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
R44h	Vertical RAM address position (EF00h)	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
R45h	Horizontal RAM address start position (0000h)	0	1	0	0	0	0	0	0	0	HSA8	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R46h	Horizontal RAM address end position (013Fh)	0	1	0	0	0	0	0	0	0	HEA8	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
R48h	First window start (0000h)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	First window end (00EFh)	0	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Ah	Second window start (0000h)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	Second window end (00EFh)	0	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Eh	Set GDDRAM X address counter (0000h)	0	1	0	0	0	0	0	0	0	XAD8	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
R4Fh	Set GDDRAM Y address counter (0000h)	0	1	0	0	0	0	0	0	0	0	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0

Note: In R01h, bits REV, BGR, RL, CM will override the corresponding hardware pins settings.
Setting R28h as 0x0006 is required before setting R25h and R29h registers.

7.0 Optical Characteristics

Items	Symbol	Condition	Min	Typ	Max	Unit	Remark
Response Time	Tr + Tf		-	35	50	ms	Note5
Contrast Ratio	Cr	$\Theta = 0^\circ$ $\emptyset = 0^\circ$ $T_a = 25^\circ\text{C}$	150	300	-	-	Note4
Brightness			250	300	-	Cd/m ²	
Uniformity	U		75	80		%	
Viewing Angle	$\theta_3 = 90$	CR>10	35	45	-	°	Note3
	$\theta_9 = 270$		35	45	-		
	$\theta_{12} = 0$		15	25	-		
	$\theta_6 = 180$		35	45	-		
CIE (X, Y) Chromaticity	White	X_w	$\Theta = 0^\circ$ $\emptyset = 0^\circ$ $T_a = 25^\circ\text{C}$	-	0.307	-	Note6
		Y_w		-	0.328	-	

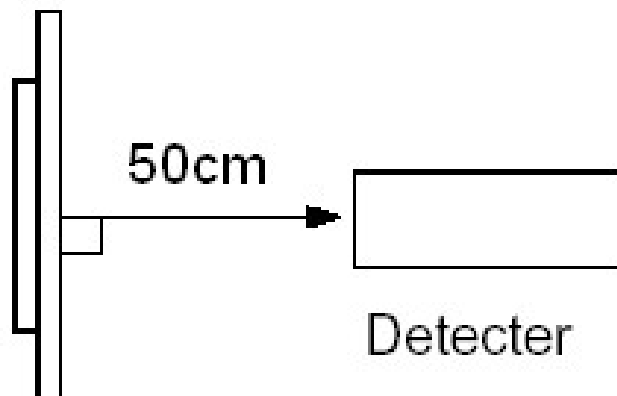
Note: The parameter is slightly changed by temperature, driving voltage and material

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705 (Φ8mm)

Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: $T_a=25^\circ\text{C}$.
- Adjust operating voltage to get optimum contrast at the center of the display.

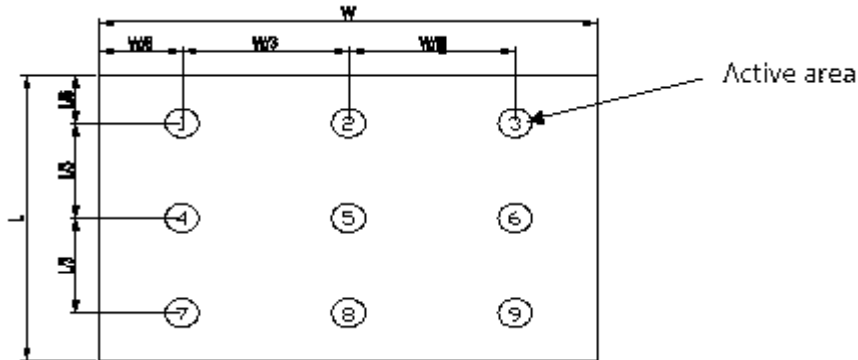
Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.



Note 2: The luminance uniformity is calculated by using following formula.

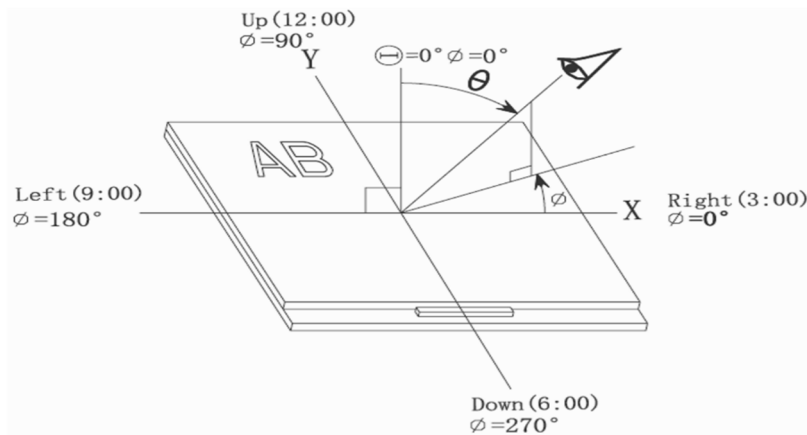
$$\Delta Bp = Bp (\text{Min.}) / Bp (\text{Max.}) \times 100 (\%)$$

$Bp (\text{Max.})$ = Maximum brightness in 9 measured spots
 $Bp (\text{Min.})$ = Minimum brightness in 9 measured spots.

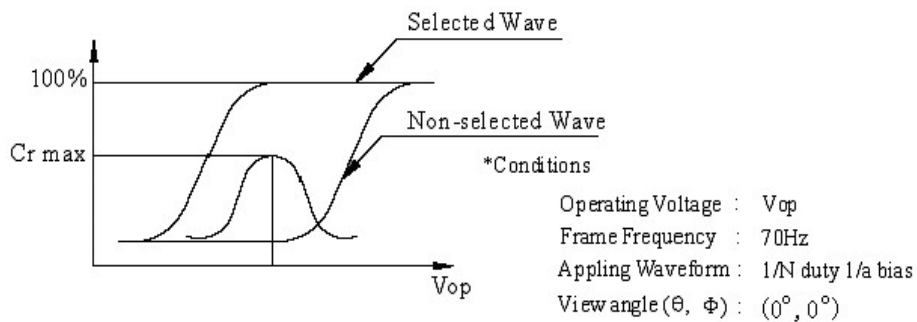


Note 3: The definition of viewing angle:

Refer to the graph below marked by θ and ϕ



Note 4: Definition of contrast ratio. (Test LCD using DMS501)

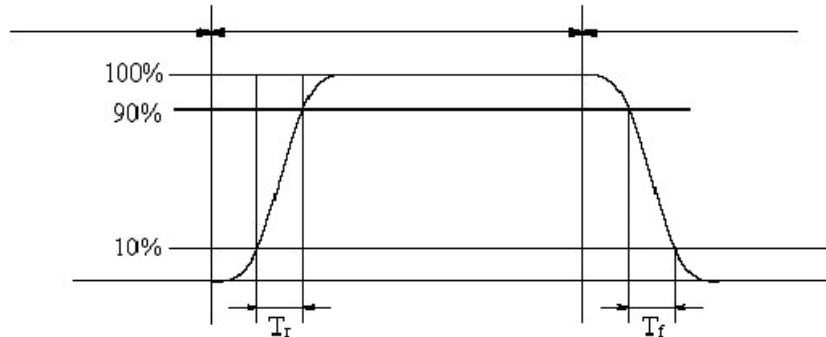


$$\text{Contrast ratio (Cr)} = \frac{\text{Brightness of selected dots}}{\text{Brightness of non-selected dots}}$$

Note 5: Definition of Response time. (Test LCD using DMS501):

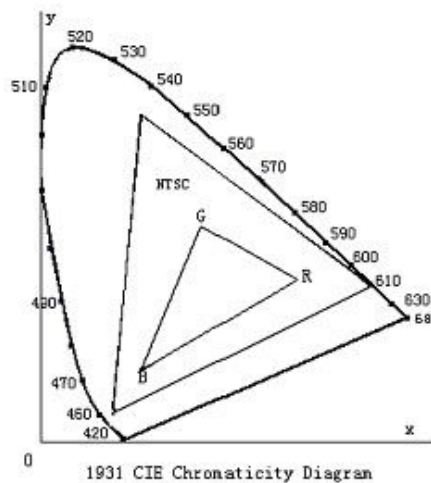


The output signals of photo detector are measured when the input signals are changed from “black” to “white” (falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



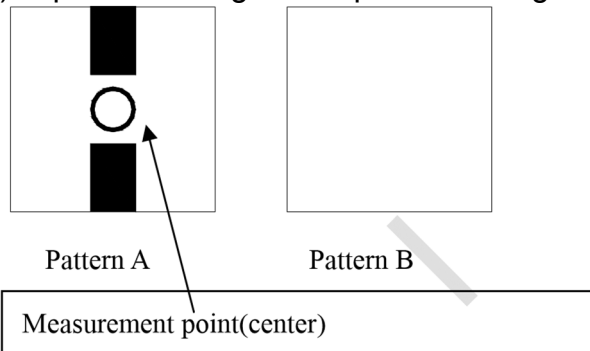
The Definition of response time

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.



Note 7: Definition of cross talk.

$$\text{Cross talk ratio (\%)} = [\text{pattern A Brightness} - \text{pattern B Brightness}] / \text{pattern A}$$



$$\text{Electric volume value} = 3F \pm 3\text{Hex}$$



8.0 Reliability Test Condition

Item		Test Condition
Operating	High Temperature	70degC, 240 hrs
	Low Temperature	-20degC,240 hrs
Storage	High Temperature	80degC, 240hrs and recovery for 2hrs
	Low Temperature	-30degC, 240hrs and recovery for 2hrs
	High Temperature and High Humidity	50degC, 90%RH, 240hrs and recovery for 2 hrs
Thermal	Cycle	RT → 20degC → Rt → 70degC → RT 0min 30min 5min 30min 5min 50 cycles (Power off)
	Shock	RT → 20degV → 70degC 0min 30min 30min 50 cycles (Power off)

Note: Rt means Room temperature

9.0 Inspection Criteria

No	Defect	Definition of defect	Inspection Criteria												
1	a) Definition of dot	<p>The size of defective dot over 1/2 of whole is regards as one defective dot.</p> <p>Smaller than 1/2 Larger than 1/2</p> <p>'No dot defect' (ignore) '1 dot defect' (counted)</p>	<p>A – Viewing Area B – Outside viewing area</p>												
	b) Bright Dot	Dot appear bright and unchanged in size when LCD panel is displaying black pattern	<table border="1"> <thead> <tr> <th>Defect</th> <th>A</th> <th>B</th> </tr> </thead> <tbody> <tr> <td>Bright Dot</td> <td>1</td> <td rowspan="3">NC</td> </tr> <tr> <td>Dark Dot</td> <td>2</td> </tr> <tr> <td>Total</td> <td>3</td> </tr> </tbody> </table> <p>NC – Not Count</p>	Defect	A	B	Bright Dot	1	NC	Dark Dot	2	Total	3		
	Defect	A		B											
	Bright Dot	1	NC												
Dark Dot	2														
Total	3														
c) Dark Dot	Dot appear dark and unchanged in size when LCD panel is displaying pure color (RED, GREEN or BLUE) pattern														
d) 2 dot adjacent	<p>1 pair = 2 dots</p> <p>Type 1 Type 2</p> <p>Type 3 or Type 3</p>	<table border="1"> <thead> <tr> <th>Defect</th> <th>Acc. Count</th> </tr> </thead> <tbody> <tr> <td>2 Bright dot Adjacent</td> <td>0</td> </tr> <tr> <td>2 Dark dot Adjacent</td> <td>1</td> </tr> </tbody> </table>	Defect	Acc. Count	2 Bright dot Adjacent	0	2 Dark dot Adjacent	1							
Defect	Acc. Count														
2 Bright dot Adjacent	0														
2 Dark dot Adjacent	1														
2	<p>Black spot White Spot Bright spot Pin Hole Foreign Particle</p>	<p>-Black/Dark/Bright Spot is points on display which appear dark/bright and usually result from contamination - These defect do not vary in size intensity (contrast) when kontras is varied.</p> <p>$D = \frac{a+b}{2}(\text{mm})$</p>	<table border="1"> <thead> <tr> <th>Defect Category</th> <th>A</th> <th>B</th> </tr> </thead> <tbody> <tr> <td>$D \leq 0.10$</td> <td>NC</td> <td rowspan="4">NC</td> </tr> <tr> <td>$0.10 \leq D \leq 0.15$</td> <td>2</td> </tr> <tr> <td>$0.15 \leq D \leq 0.20$</td> <td>1</td> </tr> <tr> <td>$D \geq 0.2$</td> <td>0</td> </tr> </tbody> </table>	Defect Category	A	B	$D \leq 0.10$	NC	NC	$0.10 \leq D \leq 0.15$	2	$0.15 \leq D \leq 0.20$	1	$D \geq 0.2$	0
Defect Category	A	B													
$D \leq 0.10$	NC	NC													
$0.10 \leq D \leq 0.15$	2														
$0.15 \leq D \leq 0.20$	1														
$D \geq 0.2$	0														
3	<p>Black Line White line Particle between POL and Glass Scratch on Glass</p>		<table border="1"> <thead> <tr> <th>Defect Category</th> <th>A</th> <th>B</th> </tr> </thead> <tbody> <tr> <td>$W \leq 0.03$</td> <td>NC</td> <td rowspan="3">NC</td> </tr> <tr> <td>$0.03 \leq W \leq 0.05, L \leq 2.0$</td> <td>2</td> </tr> <tr> <td>$W \geq 0.05$</td> <td>0</td> </tr> </tbody> </table>	Defect Category	A	B	$W \leq 0.03$	NC	NC	$0.03 \leq W \leq 0.05, L \leq 2.0$	2	$W \geq 0.05$	0		
Defect Category	A	B													
$W \leq 0.03$	NC	NC													
$0.03 \leq W \leq 0.05, L \leq 2.0$	2														
$W \geq 0.05$	0														
4	<p>POL Bubble POL Dented</p>		<table border="1"> <thead> <tr> <th>Defect Category</th> <th>A</th> <th>B</th> </tr> </thead> <tbody> <tr> <td>$D \leq 0.20$</td> <td>NC</td> <td rowspan="4">NC</td> </tr> <tr> <td>$0.20 \leq D \leq 0.30$</td> <td>3</td> </tr> <tr> <td>$0.30 \leq D \leq 0.50$</td> <td>2</td> </tr> <tr> <td>$D \geq 0.5$</td> <td>0</td> </tr> </tbody> </table>	Defect Category	A	B	$D \leq 0.20$	NC	NC	$0.20 \leq D \leq 0.30$	3	$0.30 \leq D \leq 0.50$	2	$D \geq 0.5$	0
Defect Category	A	B													
$D \leq 0.20$	NC	NC													
$0.20 \leq D \leq 0.30$	3														
$0.30 \leq D \leq 0.50$	2														
$D \geq 0.5$	0														
5	<p>Mura (50% Grey)</p>		Judged by Limit sample												



10.0 Precaution and Limited Warranty

1. Handling Precautions

- a. The display panel is made of glass and polarizer. As glass is fragile. It tends to chip during handling especially on the edges. Please avoid dropping or jarring. Do not subject it to a mechanical shock of impact or by dropping it.
- b. If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance is in contact with your skin or clothes, wash it off using soap and water.
- c. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary. Do not touch the display with bare hands. This will stain the display area and degrade the insulation between terminals. Scratch and dents may occur on polarizer too.
- d. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully. Do not touch, push or rub the exposed polarizers with anything harder than a HB pencil lead (glass, tweezers, etc.). Do not put or attach anything on the display area to avoid leaving marks on it. Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizer. After products are tested at low temperature they must be warmed up in a container before coming in to contact with room temperature air.
- e. If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents
 - Isopropyl alcohol
 - Ethyl alcohol
 - Do not scrub hard to avoid damaging the display surface.
- f. Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.
 - Water
 - Ketone
 - Aromatic solvents
 - Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading. Avoid contact with oil and fats.
- g. Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.
- h. Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.
- i. Do not attempt to disassemble or process the LCD module.
- j. NC terminal should be open. Do not connect anything.
- k. If the logic circuit power is off, do not apply the input signals.
- l. Electro-Static Discharge Control. Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
 - Before removing LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential. Be sure to ground the body when handling the LCD modules.
 - Tools required for assembly, such as soldering irons, must be properly grounded. Make certain the AC power source for the soldering iron does not leak. When using an electric screwdriver to attach LCM, the screw driver should be of ground potentiality to minimize as much as possible any



transmission of electromagnetic waves produced sparks coming from the commutator of the motor.

- To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions. To reduce the generation of static electricity be careful that the air in the work environment is not too dry. A relative humidity of 50%-60% is recommended. As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.
 - The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- m. Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.
- Do not alter, modify or change the shape of the tab on the metal frame.
 - Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
 - Do not damage or modify the pattern writing on the printed circuit board.
 - Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.
 - Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
 - Do not drop, bend or twist the LCM.

2. Storage Precautions

When storing the LCD modules, the following precaution are necessary.

- a. Store them in a sealed polyethylene bag. If properly sealed, there is no need for the desiccant.
- b. Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C, and keep the relative humidity between 40%RH and 60%RH.
- c. The polarizer surface should not come in contact with any other objects.

3. Others

- a. Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.
- b. If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.
- c. To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc. Exercise care to avoid holding the following sections when handling the modules.
 - Exposed area of the printed circuit board.
 - Terminal electrode sections.

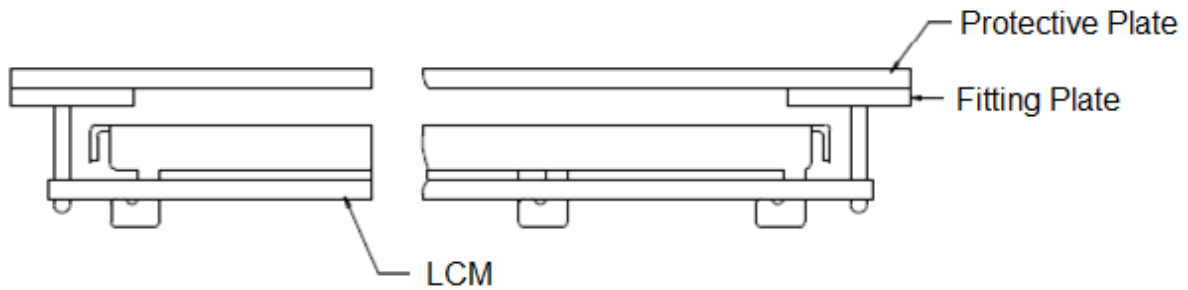
4. Using LCD Modules

a. Installing LCD Modules

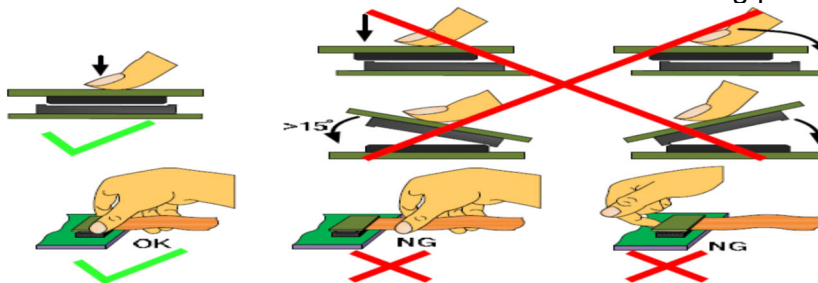
The hole in the printed circuit board is used to fix LCM as shown in the picture below.

Attend to the following items when installing the LCM.

- b. Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



- c. When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be 0.1mm.
- d. Precaution for assemble the module with BTB connector:
Please note the position of the male and female connector position, don't assemble or assemble like the method which the following picture shows



5. Precaution for soldering the LCM

	Manual soldering	Machine drag soldering	Machine press soldering
No RoHS Product	290°C ~350°C. Time: 3-5S.	330°C ~350°C. Speed: 4-8 mm/s.	300°C ~330°C. Time: 3-6S. Press: 0.8~1.2Mpa
RoHS Product	340°C ~370°C. Time: 3-5S.	350°C ~370°C. Time: 4-8 mm/s.	330°C ~360°C. Time: 3-6S. Press: 0.8~1.2Mpa

- a. If soldering flux is used, be sure to remove any remaining flux after finishing the soldering operation (This does not apply in the case of a non-halogen type of flux). It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.
- b. When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.
- c. When removing the electroluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

6. Precautions for Operation

- a. Viewing angle varies with the change of liquid crystal driving voltage (VLCD). Adjust VLCD to show the best contrast.
- b. It is recommended to drive LCD's within the specified voltage limit since over limit will cause shorter LCD life. An electrochemical reaction due to direct current causes LCD-deterioration. Avoid the use of direct current drive.



- c. Response time will be extremely delayed at lower temperature compared to room operating temperature range and on the other hand, at higher temperature LCD shows dark color in them. However those phenomena do not mean malfunction. The LCD will return to normal performance when ambient temperature revert to room condition.
- d. If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and on.
- e. A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.
- f. Input logic voltage before apply analogue high voltage such as LCD driving voltage when power on. Remove analogue high voltage before logic voltage when power off the module. Input each signal after the positive/negative voltage becomes stable.
- g. Please keep the temperature within the specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.

7. Safety

- a. It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- b. If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

8. Limited Warranty

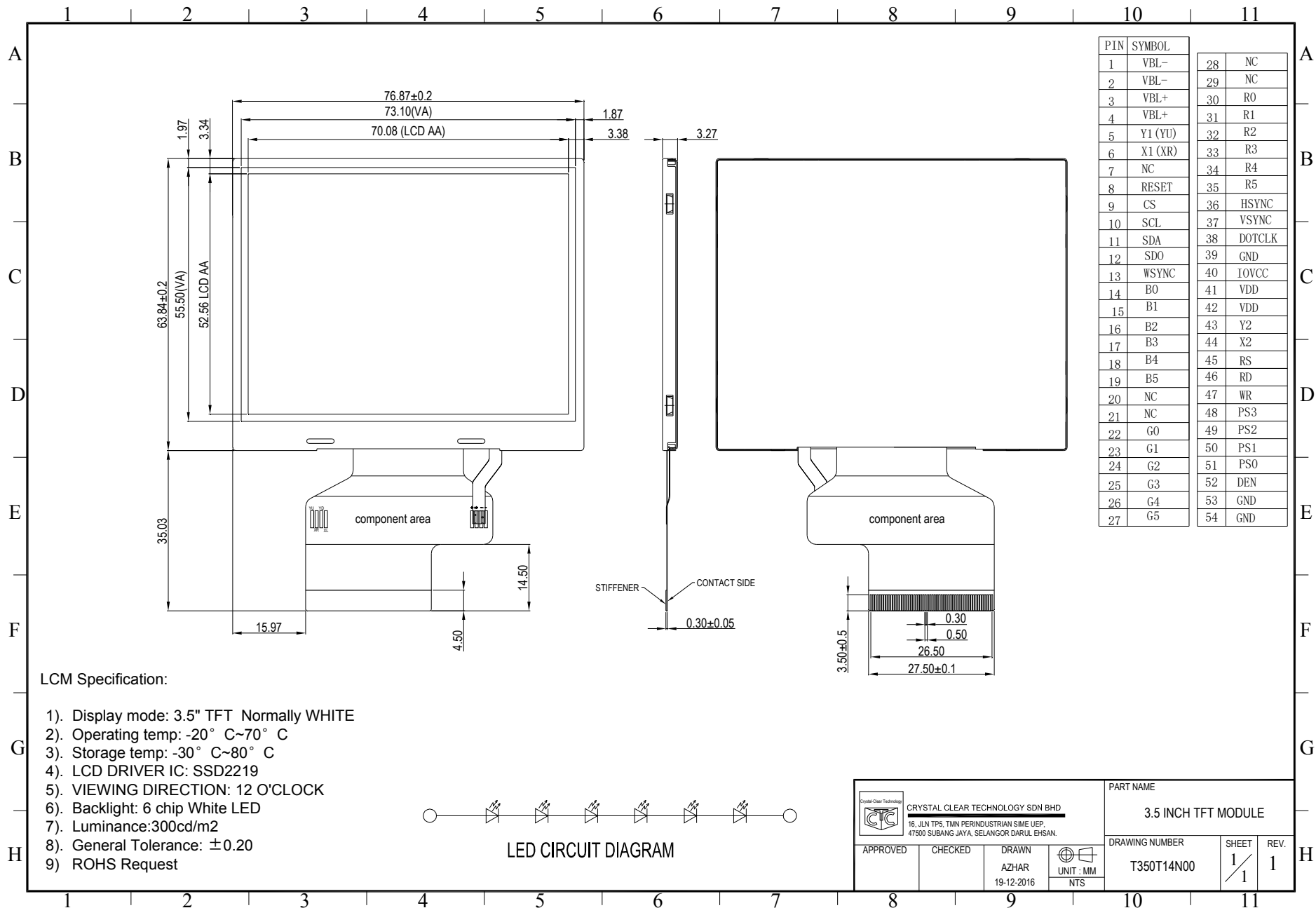
Unless otherwise agreed between Crystal Clear Technology and customer, Crystal Clear Technology will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with Crystal Clear Technology acceptance standards, for a period of one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of Crystal Clear Technology is limited to repair and/or replacement on the terms set forth above. Crystal Clear Technology will not responsible for any subsequent or consequential events.

9. Return LCM under Warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are:

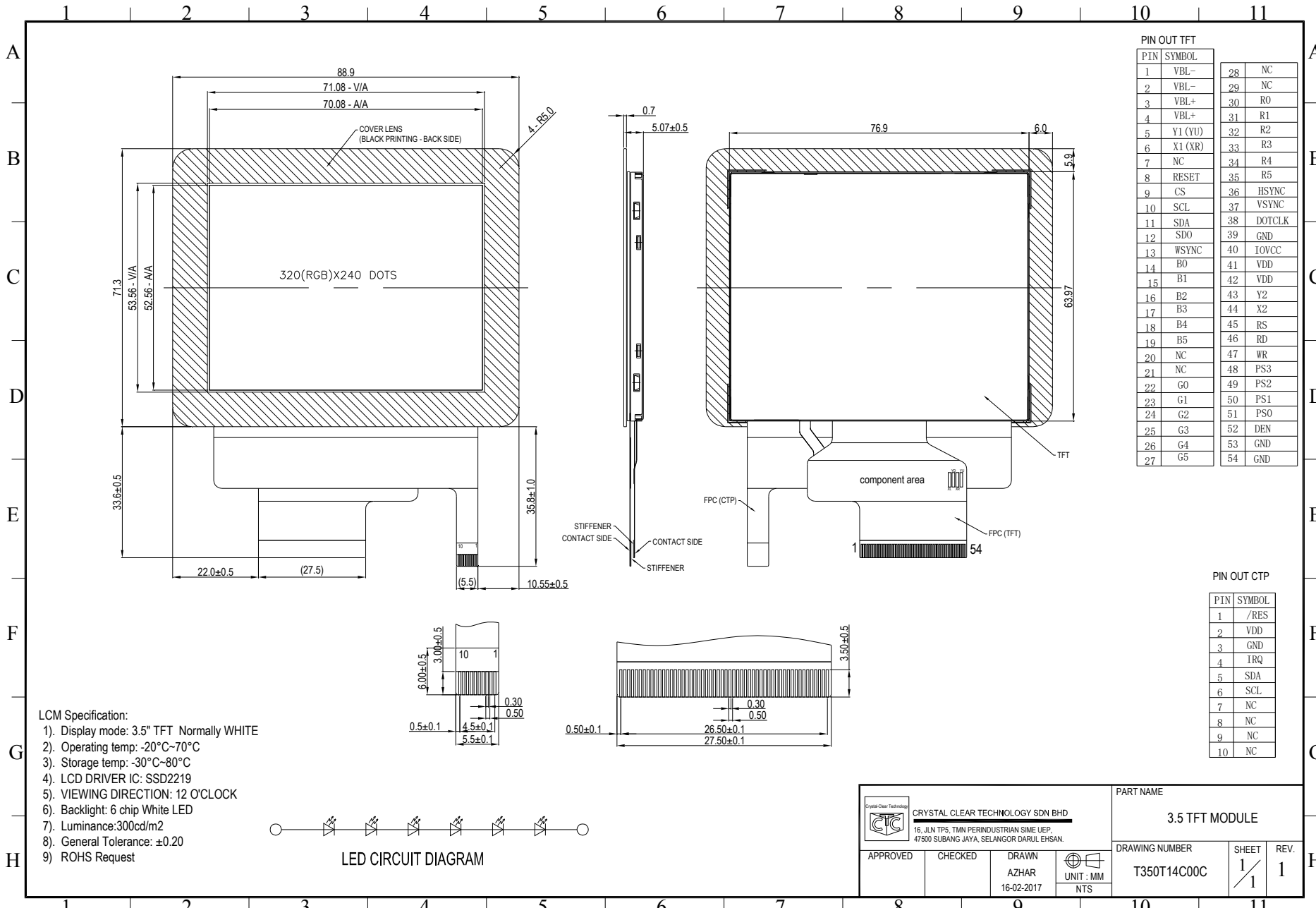
- Broken LCD glass
- PCB eyelet's damaged or modified
- PCB conductors damaged
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- Soldering to, or modifying the bezel in any manner.

Module repairs will be invoiced to customer upon mutual agreement. Modules must be returned with sufficient description of failure or defects. Any connectors or cable installed by customer must be removed completely without damaging the PCB eyelet's, conductors and terminals.



PIN	SYMBOL		
1	VBL-	28	NC
2	VBL-	29	NC
3	VBL+	30	RO
4	VBL+	31	R1
5	Y1 (YU)	32	R2
6	X1 (XR)	33	R3
7	NC	34	R4
8	RESET	35	R5
9	CS	36	HSYNC
10	SCL	37	VSYNC
11	SDA	38	DOTCLK
12	SDO	39	GND
13	WSYNC	40	IOVCC
14	B0	41	VDD
15	B1	42	VDD
16	B2	43	Y2
17	B3	44	X2
18	B4	45	RS
19	B5	46	RD
20	NC	47	WR
21	NC	48	PS3
22	G0	49	PS2
23	G1	50	PS1
24	G2	51	PS0
25	G3	52	DEN
26	G4	53	GND
27	G5	54	GND

		CRYSTAL CLEAR TECHNOLOGY SDN BHD 16, JLN TP5, TAM PERINDUSTRIAN SIME UEP, 47500 SUBANG JAYA, SELANGOR DARUL EHSAN.		PART NAME 3.5 INCH TFT MODULE	
APPROVED 	CHECKED 	DRAWN AZHAR 19-12-2016	 UNIT : MM NTS	DRAWING NUMBER T350T14N00	SHEET 1 / 1 REV. 1



PIN OUT TFT

PIN	SYMBOL		
1	VBL-	28	NC
2	VBL-	29	NC
3	VBL+	30	RO
4	VBL+	31	R1
5	Y1 (YU)	32	R2
6	X1 (XR)	33	R3
7	NC	34	R4
8	RESET	35	R5
9	CS	36	HSYNC
10	SCL	37	VSYNC
11	SDA	38	DOTCLK
12	SDO	39	GND
13	WSYNC	40	I/OVCC
14	B0	41	VDD
15	B1	42	VDD
16	B2	43	Y2
17	B3	44	X2
18	B4	45	RS
19	B5	46	RD
20	NC	47	WR
21	NC	48	PS3
22	GO	49	PS2
23	G1	50	PS1
24	G2	51	PS0
25	G3	52	DEN
26	G4	53	GND
27	G5	54	GND

PIN OUT CTP

PIN	SYMBOL
1	/RES
2	VDD
3	GND
4	IRQ
5	SDA
6	SCL
7	NC
8	NC
9	NC
10	NC

- LCM Specification:
- 1). Display mode: 3.5" TFT Normally WHITE
 - 2). Operating temp: -20°C~70°C
 - 3). Storage temp: -30°C~80°C
 - 4). LCD DRIVER IC: SSD2219
 - 5). VIEWING DIRECTION: 12 O'CLOCK
 - 6). Backlight: 6 chip White LED
 - 7). Luminance: 300cd/m2
 - 8). General Tolerance: ±0.20
 - 9). ROHS Request



		CRYSTAL CLEAR TECHNOLOGY SDN BHD 16, JLN TP5, TMM PERINDUSTRIAN SIME UEP, 47500 SUBANG JAYA, SELANGOR DARUL EHSAN.		PART NAME 3.5 TFT MODULE	
APPROVED 	CHECKED 	DRAWN AZHAR 16-02-2017	 UNIT : MM NTS	DRAWING NUMBER T350T14C00C	SHEET 1 / 1 REV. 1

Crystal Clear Technology

Product Specification

TP0106-01

Crystal Clear Technology sdn. bhd.

16Jalan TP5—Taman Perindustrian Sime UEP
47600 Subang Jaya—Selangor DE

Malaysia. T: +603 80247099 F: +603 80247098



CONTENTS

No	Title	Page
1	INTRODUCTION	3
2	GENERAL DESCRIPTION	3
3	ABSOLUTE MAXIMUM RATING	3
4	ELECTRICAL CHARACTERISTICS	4
5	PIN DEFINITION	4
6	I2C INTERFCE	4
7	APPEARANCE INSPECTION CONDITION AND METHODS	6
8	MECHANICAL SPECIFICATION	10



1.0 INTRODUCTION

The purpose of this specification is defined the general provision and quality requirement apply to 3.5 inch Capacitive Touch module integrated by Crystal Clear Technology. This document, together with the module drawing, is the highest level specification for this product. When users touch module by finger, the module can send coordinates of point at the contact point to host. The finger position information is sent to host by I2C bus which is determined by host through IRQ line.

2.0 GENERAL DESCRIPTION

This document contains the Capacitive Touch module specification. The maximum rating, characteristics, hardware, and inspection of the module are described in the subsequent sections. I2C protocol will be introduced in detail.

2.1 Touch sensor characteristics

- Technology: Use the character of capacitive among the touch electrodes on touch panel to identify the positions of touch signals
- Touch method: Ten fingers multi touch with pressure sensing
- Interface: I2C

2.2 General Specification

Item	Specification	Unit
Screen Diagonal	3.5	inch
Module Outline	76.90(H) x 63.90(V) x 0.70(T) (Excluded FPC)	mm
Touch Area	70.08(H) x 52.56(V)	mm
Controller	ST1633i	-
Cover Lens Material	None	-
Transparency	85	%

3.0 ABSOLUTE MAXIMUM RATING

Absolute Maximum rating of touch panel module is as following

Symbol	Parameter	Value	Unit
VDD	Supply Voltage	-0.3 to +6.0	V
TA	Operating Temperature	-20 to +70	°C
TSTG	Storage Temperature	-30 to +80	°C

Note: If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.



4.0 ELECTRICAL CHARACTERISTICS

DC Characteristics (unless otherwise specie, Voltage referenced to Ground, TA = -20°C to 70°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Power Supply		2.7	-	3.6	V
INML	Operating Current		-	16.1	24.0	mA
IDLE	Idle Current		-	8.1	12.2	mA
IPD	Power Down Current		-	-	20.0	uA
VIH	Logic High Input Voltage	VDD=3.3V	0.85VDD	-	-	V
VIL	Logic Low Input Voltage		-	-	0.15VDD	V
RPU	Input Pull Up Resistor		50	-	60	KΩ
IDRV	Output Driving Current	VOH=0.8VDD	6	-	-	mA
ISINK	Output Sinking Current	VOL=0.2VDD	10	-	-	mA
VLVR	Low Voltage Reset		-	-	2.3	V

5.0 PIN DEFINITION

NO.	SYMBOL	I/O	FUNCTION
1	RST	I	Sensor system global reset
2	VDD	P	Power supply
3	GND	P	Ground
4	IRQ	O	Sensor data ready request
5	SDA	I/O	I2C serial data
6	SCL	I	I2C serial clock
7	NC	-	No connect for user
8	NC	-	No connect for user
9	NC	-	No connect for user
10	NC	-	No connect for user

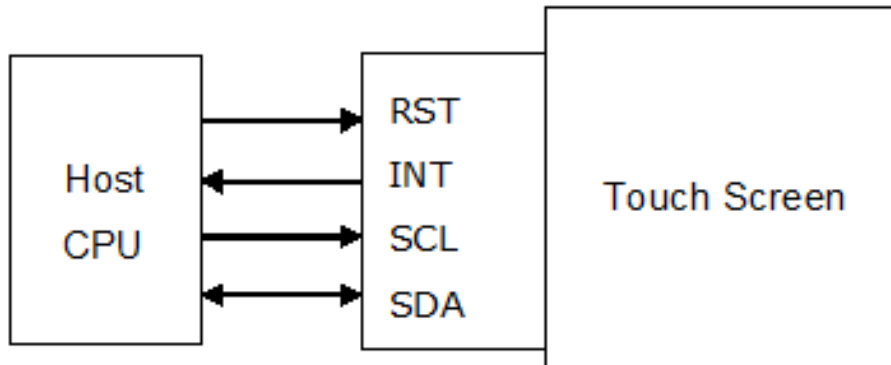
6.0 I2C INTERFACE

Touch panel is used as I2C Slave Device, I2C Slave address is 0x55

6.1 Interface Diagram

The system block diagram is as shown in below. There are three communication pins connected between CPU and Touch Panel Module which are including external interrupt INT, I2C pins SCL and SDA. The INT is active low while the touch state is calculated by Touch Panel Module and the touch information can be translated via I2C communication interface.

Touch Panel Module



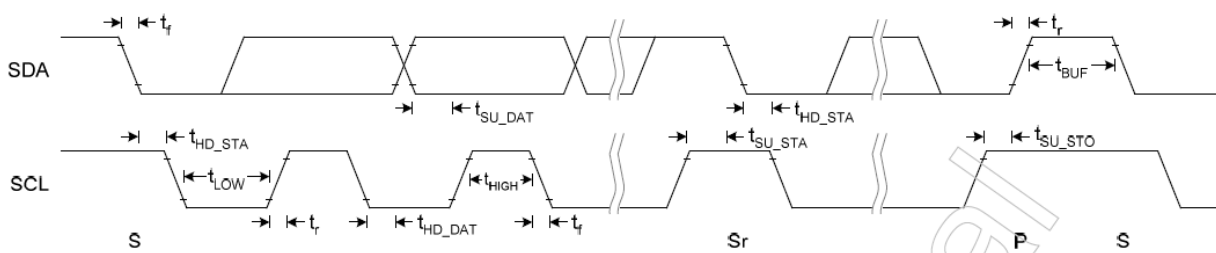
6.2 Timing Characteristic

Conditions:

VDD - GND = 3.3V

TA = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	0	-	400	kHz
t _{LOW}	Low period of the SCL clock	1.3	-	-	us
t _{HIGH}	High period of the SCL clock	0.6	-	-	us
t _f	Signal falling time	-	-	300	ns
t _r	Signal rising time	-	-	300	ns
t _{SU_STA}	Set up time for a repeated START condition	0.6	-	-	us
T _{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6	-	-	us
t _{SU_DAT}	Data set up time	100	-	-	ns
t _{HD_DAT}	Data hold time	0	-	0.9	us
t _{SU_STO}	Set up time for STOP condition	0.6	-	-	us
t _{BUF}	Bus free time between a STOP and START condition	1.3	-	-	us
C _b	Capacitive load for each bus line	-	-	400	pF



7.0 APPEARANCE INSPECTION CONDITION AND METHODS

- 7.1 Inspection distance : 25~30cm
- 7.2 Angle of inspection:
 - 7.2.1 Under black background, 1.0K- 1.5K Lux, rotate the C-TP from head on to 45° to check on defects such as foreign material, line shape, pin hole, bubble, scratches, dented and chips. (Figure 1)
 - 7.2.2 Put on light box to check on defects such as black dot, cover lens ink print scratch and pin hole. (Figure 2a or Figure 2b)

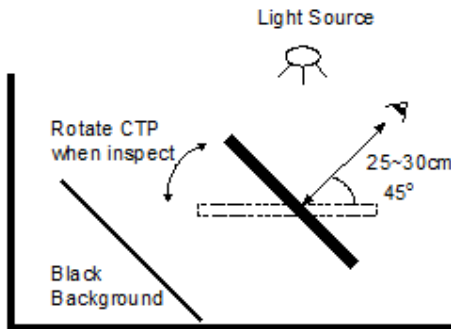


Figure 1

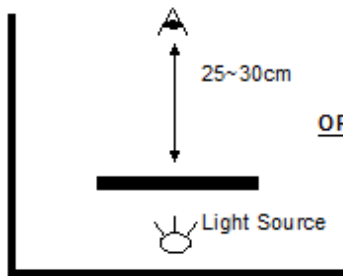


Figure 2a

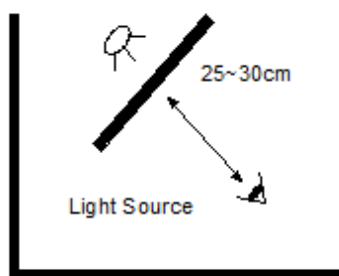


Figure 2b

For pin hole defect is determined by the size of D dot diameter, irregular dot defect is determined by $D = (\text{length} + \text{width})/2$.