Crystal Clear Technology

Product Specification

G1212X03 series

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1.0 Table of Contents

2.0 Record of revision

Rev	Date	Item	Page	Comment	Originator	Checked By
1.0	21/03/09			Initial Release	Khairiah	Azhar

3.0 General specification

Display format: Graphics 128 (w) x 128 (h) dots

Dot size: 0.33 (w) x 0.33 (h) mm

Dot pitch: 0.35 (w) x 0.35 (h) mm

View area: 50.0 (w) x 50.0 (h) mm

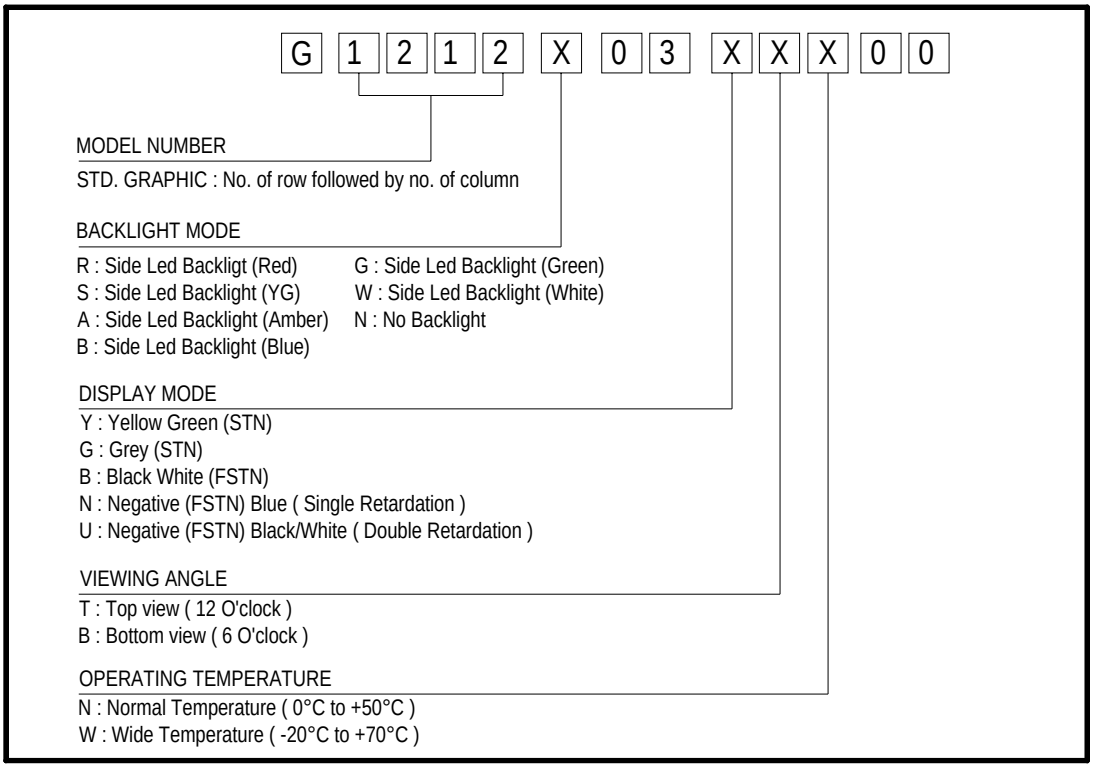
Active area: 44.78 (w) x 44.78 (h) mm

General dimensions: 73.5 (w) x 73.3 (h) x 4.5 (t) mm

Controller/Driver: ST7541i or equivalent

Interface: Serial

Driving method: 1/128 duty, 1/11 bias



4.0 Absolute maximum rating (at Vss = 0V, ambient temperature = 25°C)

NO	ITEM	SIMBOL	MIN	MAX	UNIT
1.	Operating Voltage Range	V_{DD}	-0.3	4.0	V
2.	Operating Temperature	T_{op}	Refer page 3		°C
3.	Storage Temperature	T_{st}	Refer page 3		°C

5.0 Electrical characteristics

NO	ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
1.	Operating Voltage	V_{DD}	-	-	3.3	-	V
2.	Power Supply voltage	V_{LCD}	25°C	11.5±5%			V
3.	Current Supply	I_{DD}	V_{DD} = 3.3V 4x Boosting	-	120	400	uA

5.1 Backlight Options

NO	COLOR	FORWARD VOLTAGE (V)			FORWARD CURRENT (mA)			MIN BRIGHTNESS (cd/m2) *
		Min	Typ.	Max	Min	Typ.	Max	
1.	Yellow Green	-	3.3	-	-	80	120	45
2.	White	-	3.3	-	-	60	90	200
3.	Blue	-	-	-	-	-	-	-

*Note : 1. Brightness measured at backlight surface.
2. On LCD surface, brightness is only about 10% to 15% of backlight brightness.
3. Lifetime of backlight: For YG = 50K hrs. For White, Blue = 20K hrs

6.0 Environmental requirements

NO	ITEM	CONDITION
1.	Operating Temperature	Refer page 3
2.	Storage Temperature	Refer page 3
3.	Operating Humidity	5% to 95%RH
4.	Cycle Test	0 C @ 30 min to 50 C @ 30min for 1 cycle run for 10 cycles
5.	Lifetime	50000 HOURS (excluding backlight)

Note: The background on LCD has the possibility to be changed in different temperature range.

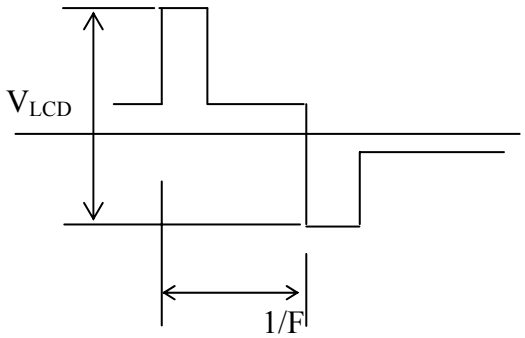
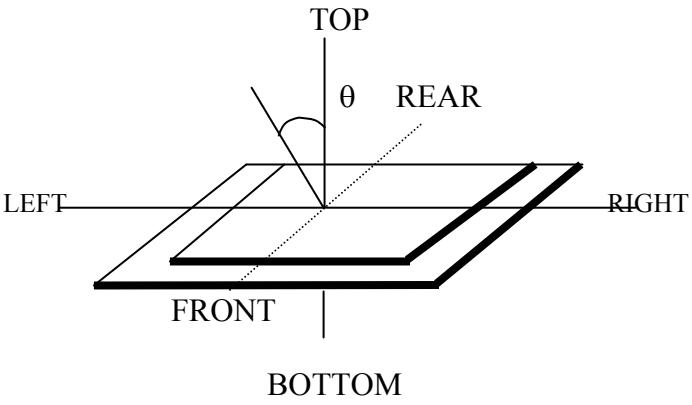
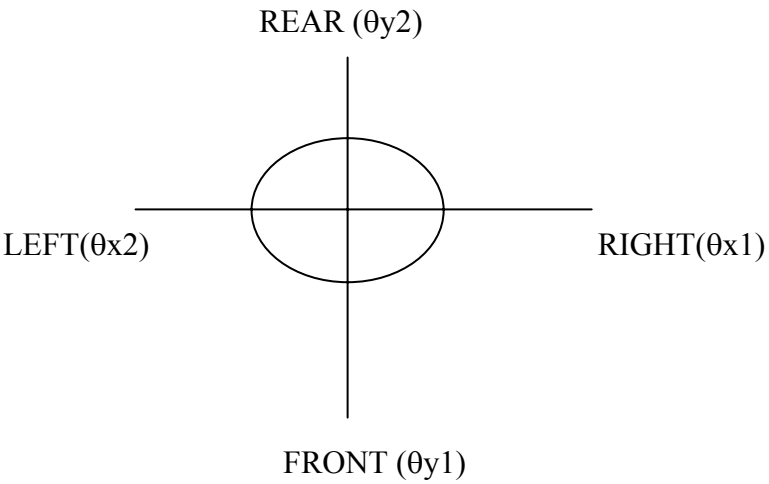
7.0 LCD specification

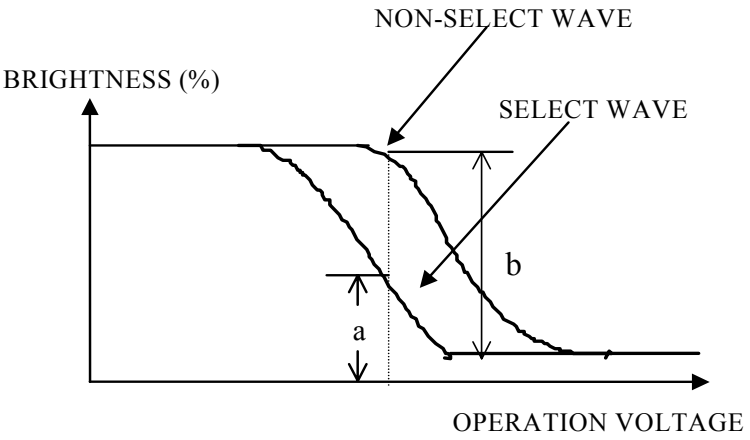
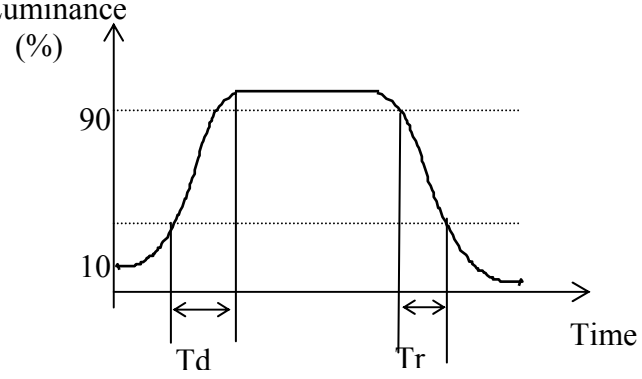
7.1 Electro-optical characteristics (at ambient temperature = 25°C)

NO	ITEM	SYMBOL	CONDITION	LCD TYPE							REF.
				STN YG	STN GREY	STN -VE BLUE	FSTN +VE B/W	FSTN –VE BLUE	FSTN -VE TRUE B/W	FSTN -VE TRI AXIS	
1	Operating Voltage (Volt)	V_{LCD}	θ = 0 Cr = max	8.0 ± 5%							7.1.1
2	Viewing Angle (Deg)	θ x 1	CR ≥ 2 V_{LCD} = 14.7V	+25	+20	+35	+25	+35	+35	+40	7.1.2
		θ x 2		-25	-20	-35	-25	-35	-40	-40	
		θ y 1		-30	-25	-35	-30	-35	-35	-50	
		θ y 2		+30	+25	+35	+30	+35	+35	+30	
3	Contrast Ratio	CR	θ = 0^0 V_{LCD} =14.7V	3.0	2.3	6.0	3.0	6.0	20	20	7.1.3
4	Response Time (msec)	Rise Time (Tr)	θ = 0^0	200							7.1.4
		Decay Time (Td)	θ = 0^0	250							

Note:

1. Viewing angle data is based on bottom view product by default. Should it be a top view product, values are then swap.
2. Contrast ratio is based on typical data when using white colour as backlight.
3. Equipment Used Eldim; Ez Contrast 120R , Spot Size = 2mm

NO	CHARACTERISTICS	DEFINITIONS
7.1.1	***Definition of Operating Voltage (V_{LCD})***	 V_{LCD} : Operating Voltage F : Frame Frequency
7.1.2	***Definition of Viewing Angle***	 

7.1.3	***Definition of Contrast Ratio***	 Contrast Ratio = Brightness of non-selected state (b) / Brightness of selected state (a) ***Conditions*** (a) Operating Voltage: V_{LCD} (b) Temperature: 25°C (c) Viewing Angle, $\theta = 0^{o}$
7.1.4	*Response Time*	Luminance (%)  Tr: Measured between 10% and 90% of LCD segment maximum response with $V_{ON.}$ Td: With voltage switches to zero and the instant LCD segment reaches 10% of its maximum response.

8.0 Interface

8.1	***Display Driver***	ST7541 OR EQUIVALENT	
8.3	**Pin No**	**Symbol**	**Description**
	1	A	Backlight Supply
	2	K	Backlight Ground
	3	RST	Reset pin
	4	SDA	IIC Data bus
	5	SCL	IIC Clock bus
	6	VDD	Logic Power Supply
	7	VSS	Ground
	8	VOUT	Booster Output Voltage
	9	V4	LCD Driving Voltage
	10	V3	LCD Driving Voltage
	11	V2	LCD Driving Voltage
	12	V1	LCD Driving Voltage
	13	V0	LCD Driving Voltage

9.0 Functional Descriptions

9.1.1 Serial Interface

3-Line / 4-Line (PS[2:0] = "000" or "010")

When the ST7541 is active (CSB="L"), serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select (A0) Pin, based on the setting of PS1. When the A0 pin is used (PS1 = "H"), data is display data when A0 is high, and command data when A0 is low. When A0 is not used (PS1 = "L"), the LCD Driver will receive command from MCU by default. If messages on the data pin are data rather than command, MCU should send Data Direction command (11101000) to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are sent, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string is handled as command data.

In 3-Line mode, default message from MCU is command, the 2 bytes command of **Set Data Direction & Display Data Length** must be set before display data send from MCU, after the display data is sent over, the next message is turned to be command.

Serial mode	PS0	PS1	PS2	CSB	A0
3-Line SPI mode	L	L	L	CSB	No used
4-Line SPI mode	L	H	L	CSB	Used
IIC SPI mode	L	L	H	CSB	No Used

If A0 is not used it must be fixed either "H" or "L"

4-Line SPI Mode (PS0 = "L", PS1 = "H", PS2 = "L")

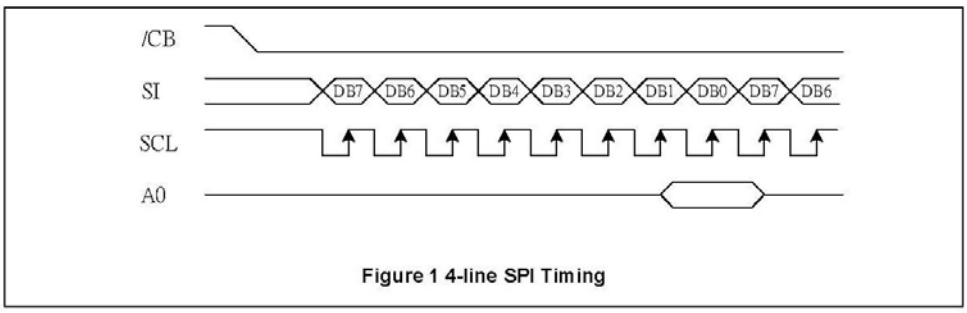
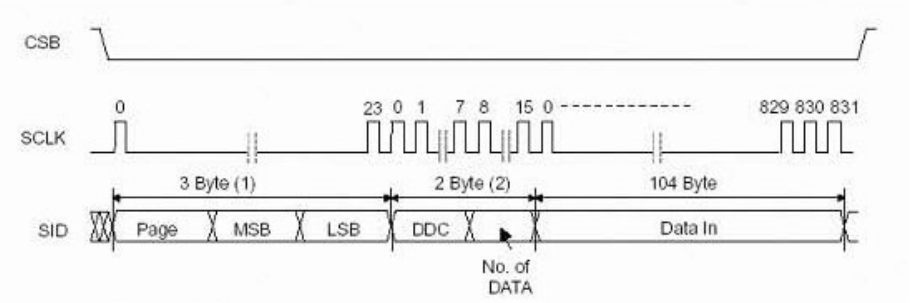


Figure 1 4-line SPI Timing

3-Line SPI Mode (PS0 = "L", PS1 = "L" ,PS2= "L")

To write data to the DDRAM, send Data Direction Command in 3-Line SPI mode. Data is latched at the rising edge of SCLK. And the DDRAM column address pointer will be increased by one automatically.



(1) Set Page and Column Address.

Set Page Address	: 1 0 1 1	P3 P2 P1 P0
Set Column Address MSB	: 0 0 0 1	0 Y7 Y6 Y5
Set Column Address LSB	: 0 0 0 0	Y4 Y3 Y2 Y1

(2) Set DDC (Data Direction Command) and No. of Data Bytes.

Set Data Direction Command (For SPI mode Only):

1 1 1 0 1 0 0 0

Set No. of Data Bytes : D7 D6 D5 D4 D3 D2 D1 D0

(3) This figure is example for 104 Data bytes to be transferred.

Figure 2. 3-pin SPI Timing (RS is not used)

This command is used in 3-Line SPI mode only. It will be two continuous commands, the first byte controls the data direction and informs the LCD driver the second byte will be number of data bytes will be write. After these two commands sending out, the following messages will be data. If data is stopped in transmitting, it is not valid data.

New data will be transferred serially with most significant bit first.

NOTE: In spite of transmission of data, if CSB will be disable, state terminates abnormally. Next state is initialized.

9.1.2 IIC Interface (PS0= 'L', PS1 = 'L', PS2 = 'H')

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.

The IIC Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 3.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 4.

SYSTEM CONFIGURATION

The system configuration is illustrated in Figure 5.

· Transmitter: the device, which sends the data to the bus

· Receiver: the device, which receives the data from the bus

· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer

· Slave: the device addressed by a master

· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message

· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted

· Synchronization: procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge, after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge, related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Figure 6.

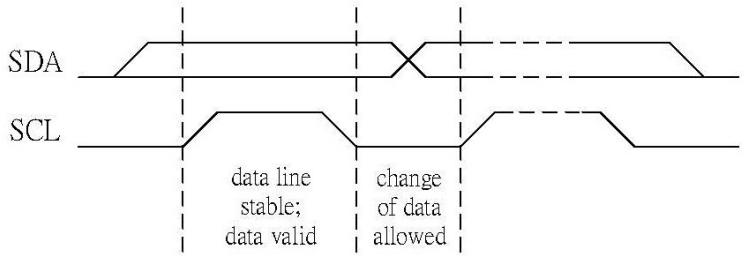


Figure 3 Bit transfer

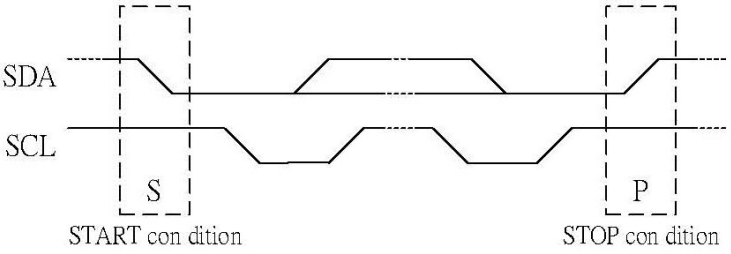


Figure 4 Definition of START and STOP conditions

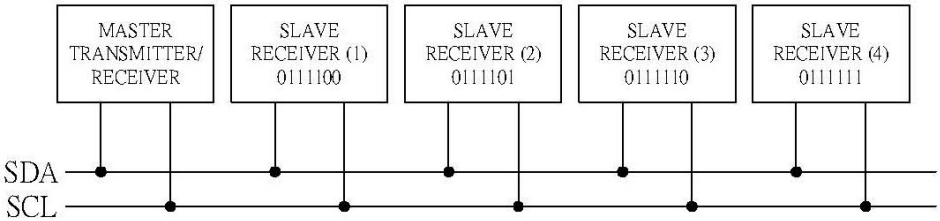


Figure 5 System configuration

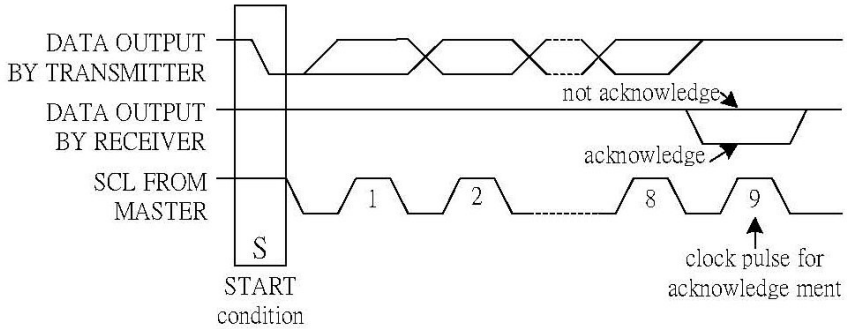


Figure 6 Acknowledgement on the 2-line Interface

9.1.3 IIC Interface Protocol

The ST7541 supports command, data write addressed slaves on the bus.

Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100,0111101, 0111110 and 0111111) are reserved for the ST7541. The least significant bit of the slave address is set by connecting the input SA0 and SA1 to either logic 0 (Vss) or logic 1 (VDD).

The IIC Interface protocol is illustrated in Figure 7.

The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.

A command word consists of a control byte, which defines Co and A0, plus a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7541 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC INTERFACE-bus master issues a STOP condition (P).If the R/W bit is set to logic 1 the chip will output data immediately after the slave address if the A0 bit, which was sent during the last write access, is set to logic 0. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

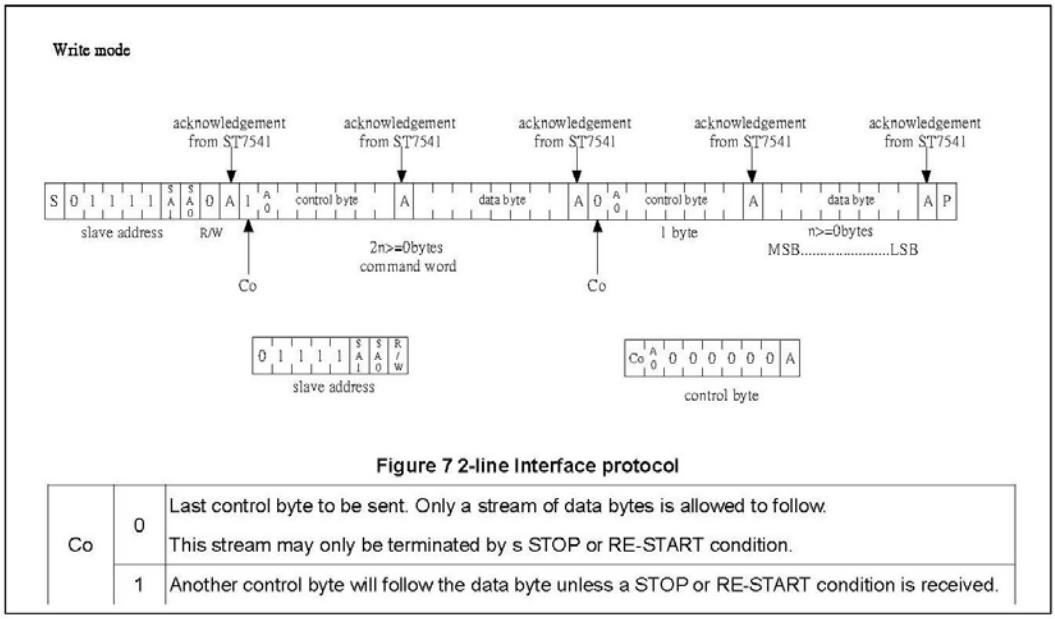


Figure 7 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

Busy Flag

The Busy Flag indicates whether the ST7541 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The ST7541 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure 8. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Figure 9. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

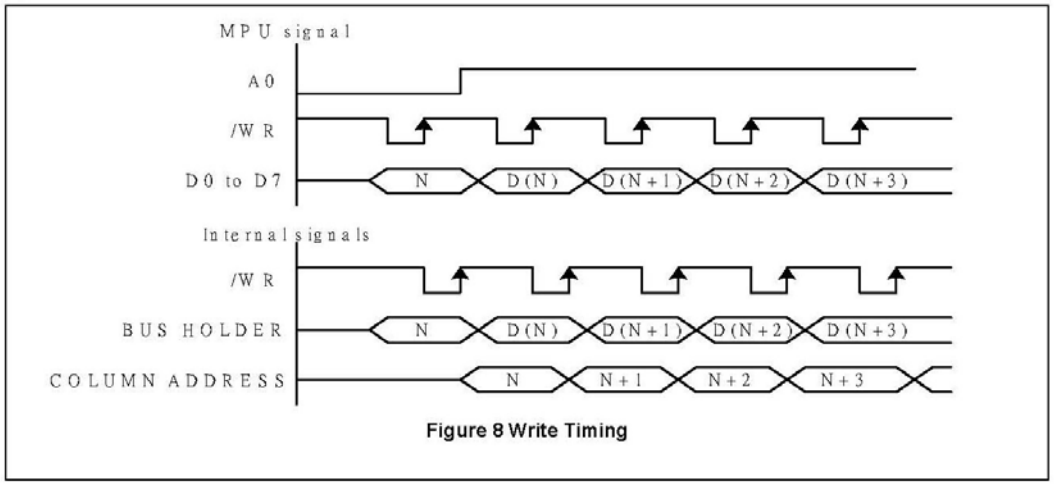


Figure 8 Write Timing

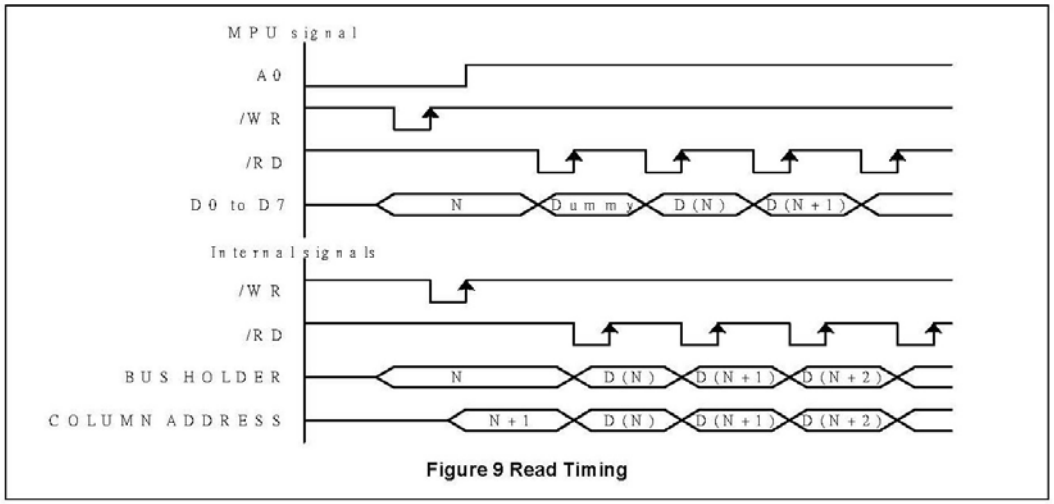


Figure 9 Read Timing

9.2 Oscillator

This is on-chip Oscillator without external resistor. When the internal oscillator is used, this pin must connect to VDD; when the external oscillator isused, this pin could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

9.3 Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 128-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 11.

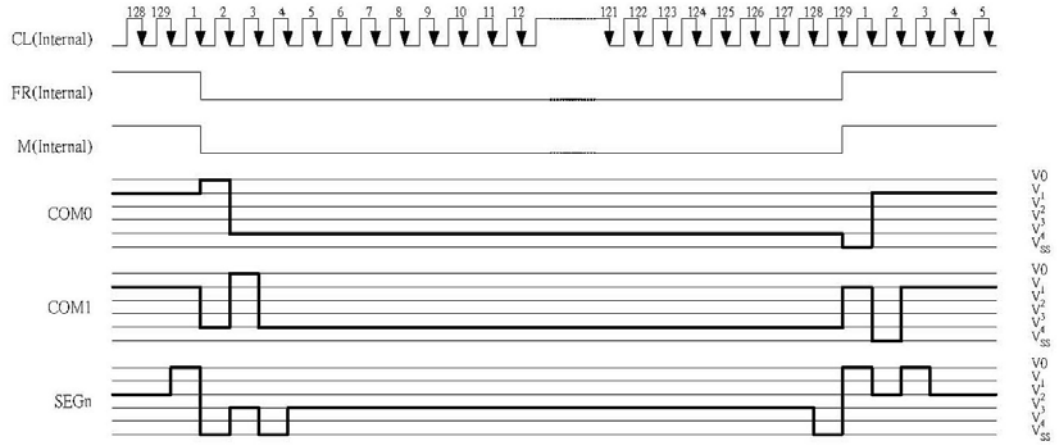


Figure 11 2-frame AC Driving Waveform (Duty Ratio: 1/129)

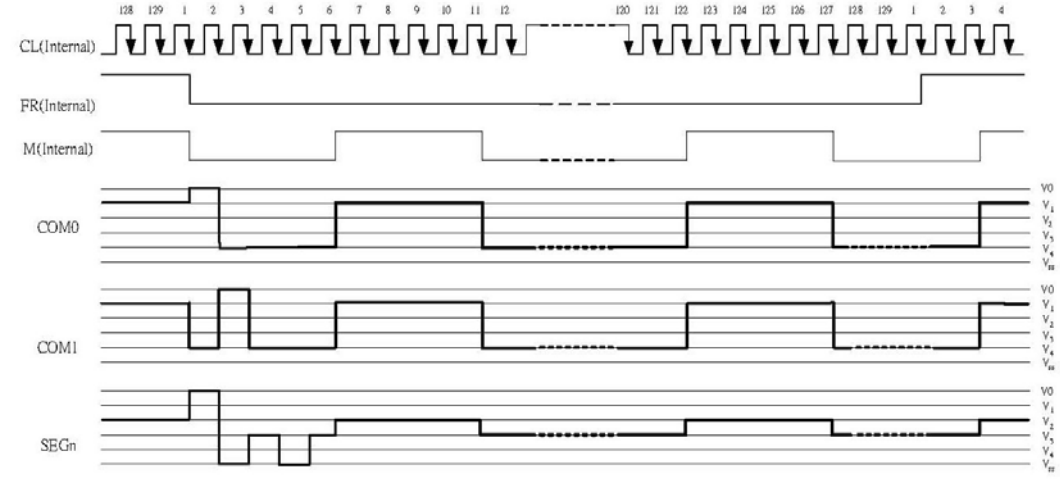


Figure 12 N-Line Inversion Driving Waveform (N=5,Duty Ratio=1/129)

9.4 Read/Write Timing Characteristic

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

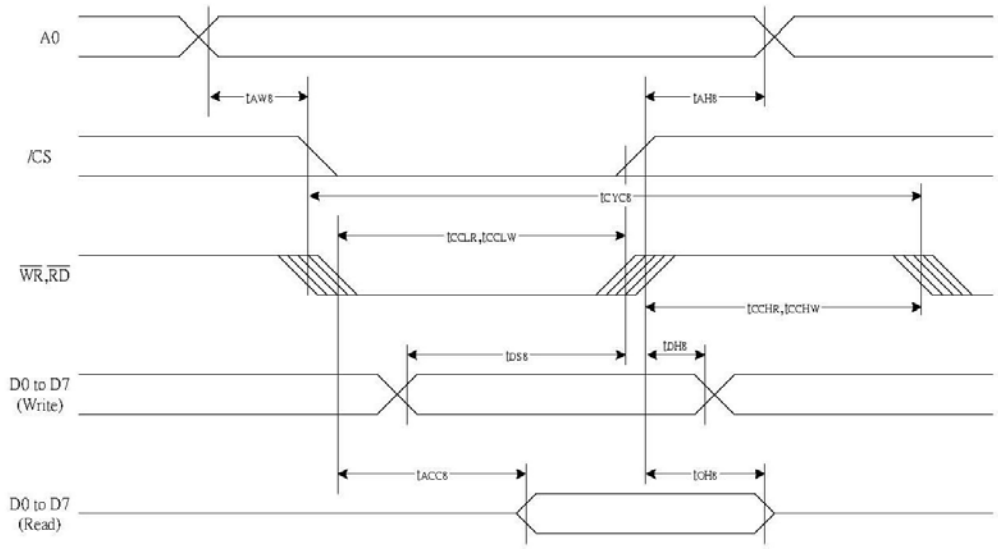


Figure 29

(VDD = 3.3V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Data hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

(VDD = 2.7 V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		400	—	
Enable L pulse width (WRITE)	WR	tCCLW		220	—	
Enable H pulse width (WRITE)		tCCHW		180	—	
Enable L pulse width (READ)	RD	tCCLR		220	—	
Enable H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Data hold time		tDH8		15	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	10	100	

(VDD = 1.8V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		640	—	
Enable L pulse width (WRITE)	WR	tCCLW		360	—	
Enable H pulse width (WRITE)		tCCHW		280	—	
Enable L pulse width (READ)	RD	tCCLR		360	—	
Enable H pulse width (READ)		tCCHR		280		
WRITE Data setup time	D0 to D7	tDS8		80	—	
WRITE Data hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

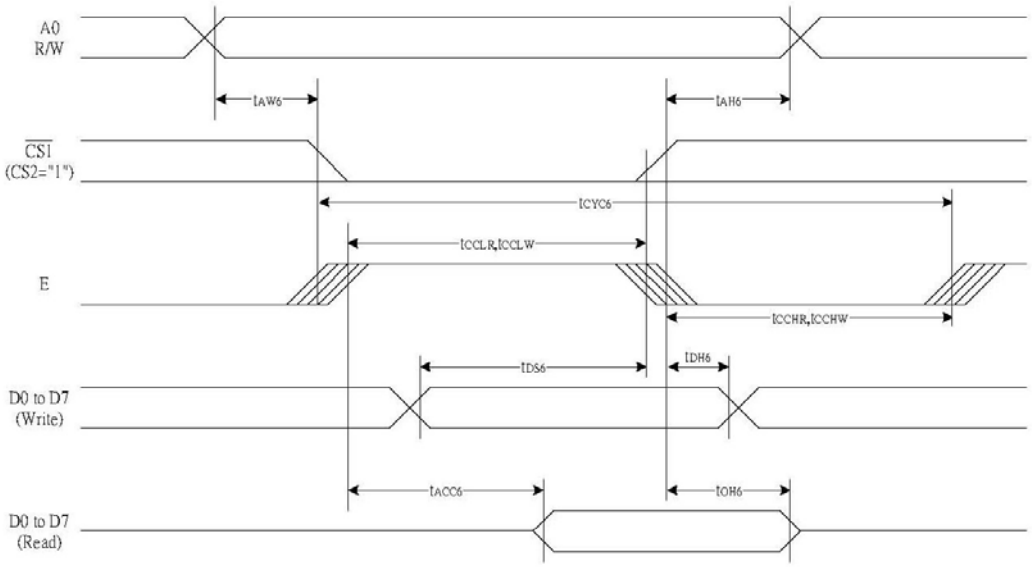


Figure 30

(V_{DD} = 3.3 V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	WR	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)	RD	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

(VDD = 2.7V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		400	—	
Enable L pulse width (WRITE)	WR	tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)	RD	tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Data hold time		tDH6		15	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	10	100	

(VDD =1.8V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		640	—	
Enable L pulse width (WRITE)	WR	tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)	RD	tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
WRITE Data setup time	D0 to D7	tDS6		80	—	
WRITE Data hold time		tDH6		30	—	
READ access time		tACC6	CL = 100 pF	—	240	
READ Output disable time		tOH6	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being "L" and E.

SERIAL INTERFACE(4-Line Interface)

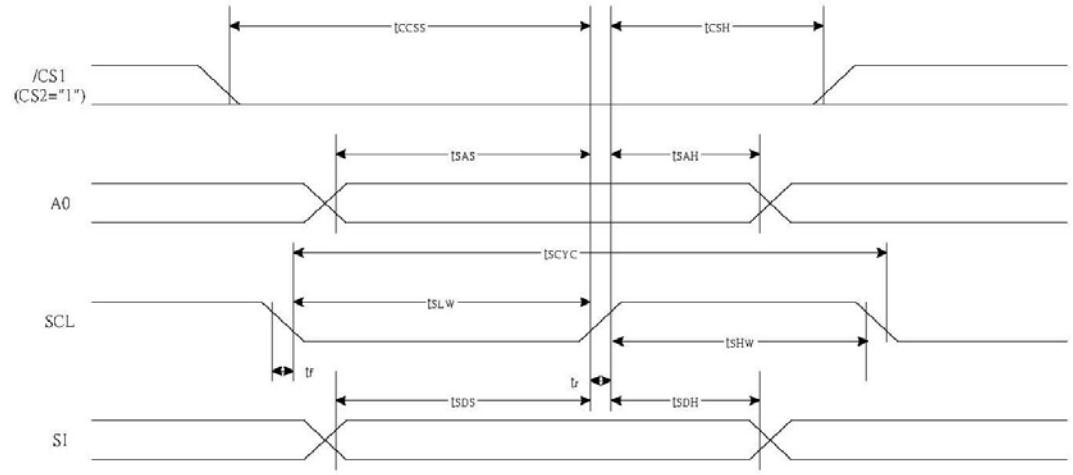


Figure 31

(V_{DD}=3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		50	—	ns
SCL "H" pulse width		tSHW		25	—	
SCL "L" pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		40	—	

(V_{DD}=2.7V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		100	—	ns
SCL "H" pulse width		tSHW		50	—	
SCL "L" pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		60	—	

(V_{DD}=1.8V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

SERIAL INTERFACE(3-Line Interface)

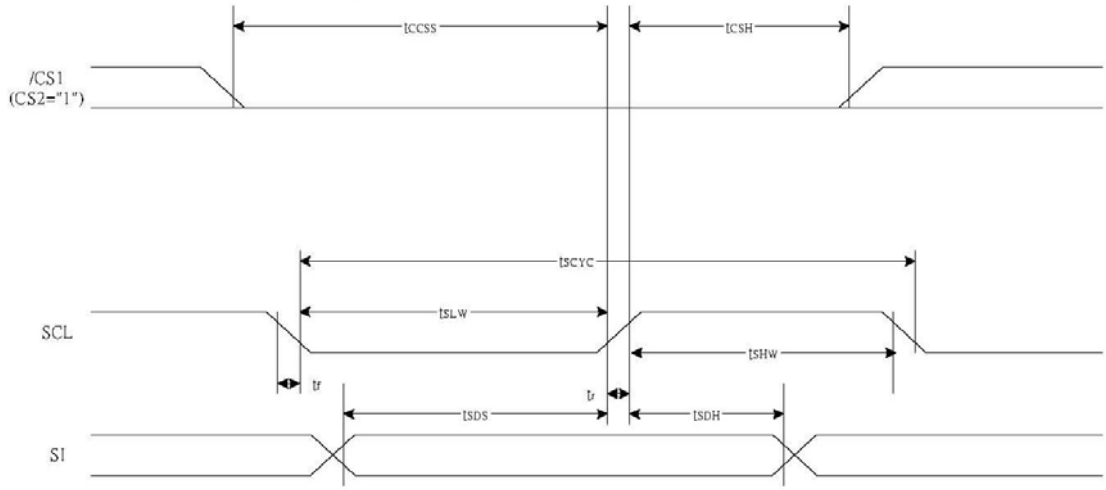


Figure 32

(V_{DD}=3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		50	—	ns
SCL "H" pulse width		tSHW		25	—	
SCL "L" pulse width		tSLW		25	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		40	—	

(V_{DD}=2.7V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		100	—	ns
SCL "H" pulse width		tSHW		50	—	
SCL "L" pulse width		tSLW		50	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		60	—	

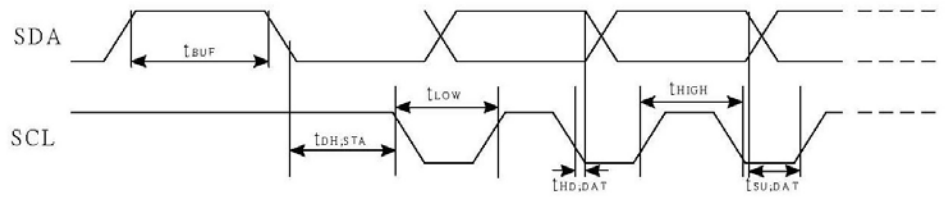
(V_{DD}=1.8V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL "H" pulse width		tSHW		80	—	
SCL "L" pulse width		tSLW		80	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

SERIAL INTERFACE(IIC Interface)



(V_{DD}=3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		-	400	kHZ
SCL clock low period	SCL	TLOW		1.3	-	us
SCL clock high period	SCL	THIGH		0.6	-	us
Data set-up time	SI	TSU;Data		100	-	ns
Data hold time	SI	THD;Data		0	0.9	us
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Setup time for a repeated START condition	SI	TSU;SUA		0.6	-	us
Start condition hold time	SI	THD;STA		0.6	-	us
Setup time for STOP ondition		TSU;STO		0.6	-	us
Tolerable spike width on bus		TSW		-	50	ns
BUS free time between a STOP and StART condition	SCL	TBUF		1.3		us

RESET TIMING

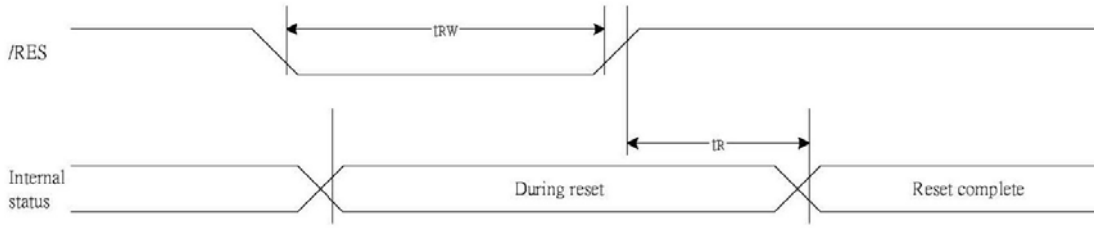


Figure 33

(VDD = 3.3V , Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	us
Reset "L" pulse width	RESB	tRW		1	—	—	us

(VDD = 2.7V , Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.5	us
Reset "L" pulse width	RESB	tRW		1.5	—	—	us

(VDD = 1.8V , Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset "L" pulse width	RESB	tRW		2.0	—	—	us

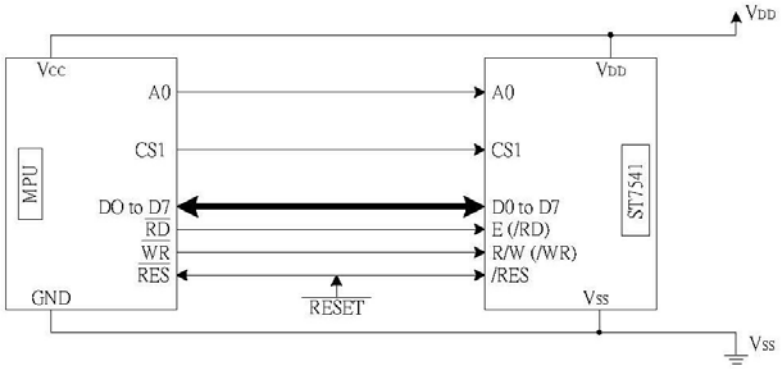
9.5 Application Circuit

THE MPU INTERFACE (REFERENCE EXAMPLES)

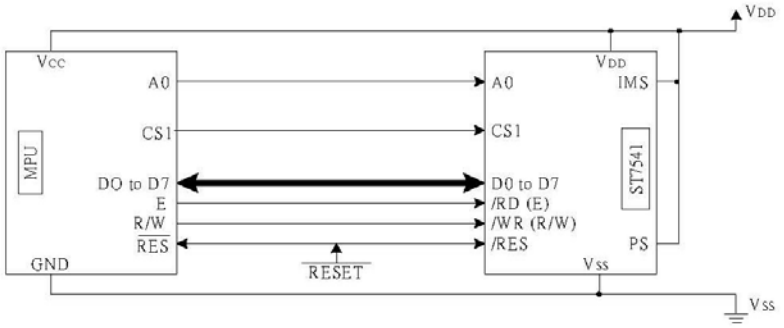
The ST7541 Series can be connected to either60X86 Series MPUs or to 6800Swries MPUs. Moreover, using the serial interface it is possible to operate the ST7541 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7541 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

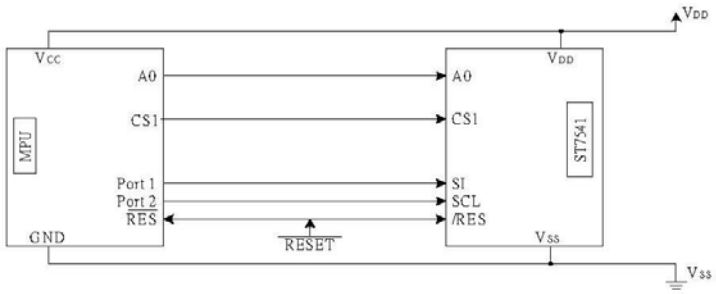
(1) 8080 Series MPUs



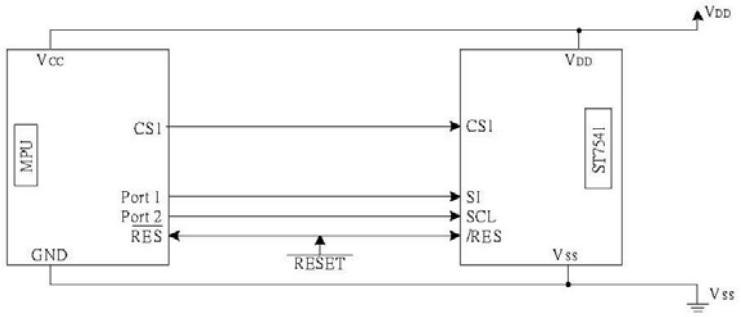
(2) 6800 Series MPUs



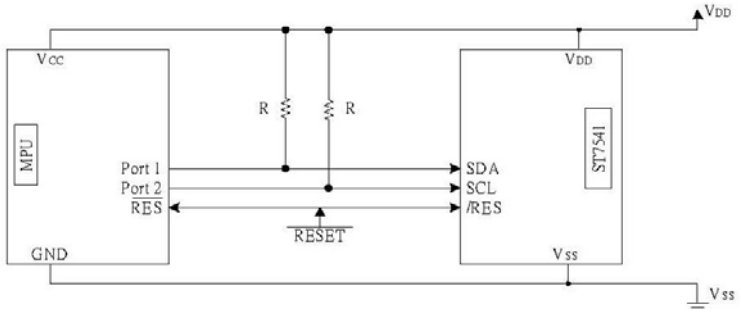
(3) Using the Serial Interface (4-line interface)



(4) Using the Serial Interface (3-line interface)

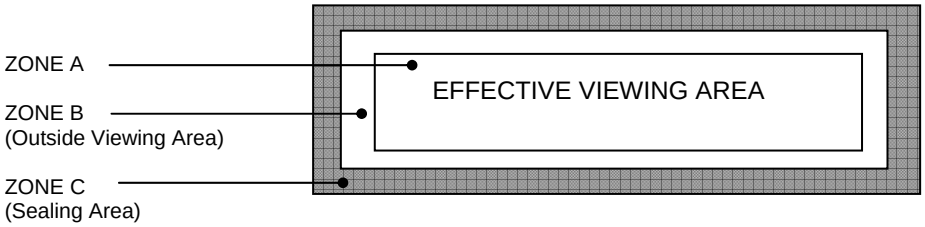


(5) Using the Serial Interface (IIC interface)



10.0 Quality Assurance

10.1 ZONE DEFINITION

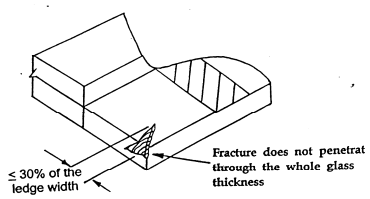
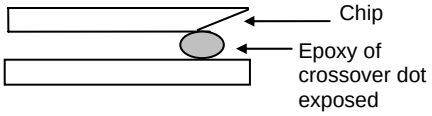
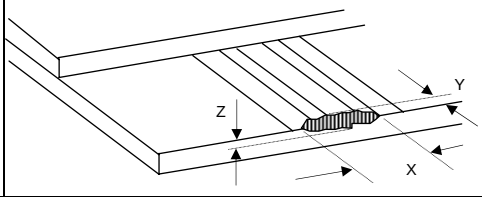
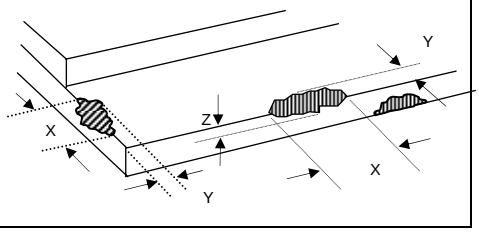


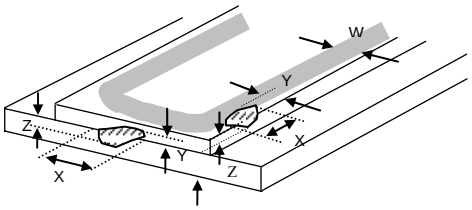
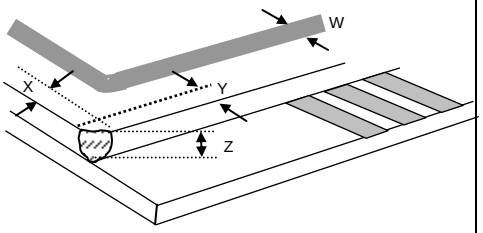
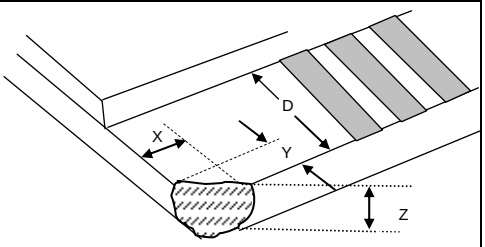
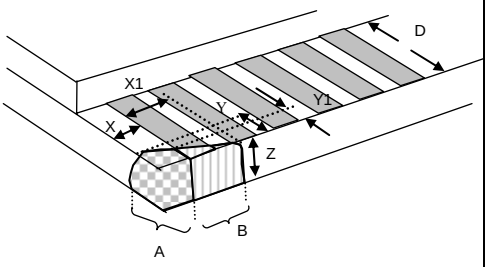
10.2 REJECTION CRITERIA

10.2.1 DIMENSIONAL DEFECTS

Defect Category	Defect Description	Criterion	Drawing Specification
Glass Size	Dimensions of LCD, do not conform to the drawing	Reject	Refer to LCD Physical Dimension Drawing
Perimeter Seal Extension	Perimeter seal epoxy enters the effective viewing area	Reject	
End Seal Size	Size of end seal does not meet drawing specification	Reject	Refer to LCD Physical Dimension Drawing

10.2.2 VISUAL DEFECTS

Defect Category	Defect Description	Criterion	Drawing Specification
Fracture	A type of glass breakage containing running cracks. Inspectors should attempt to remove it with fingernail. If removed, evaluate as chip	Reject – if the size is ≥ 30% of the contact ledge width.	
Defect Category	Defect Description	Criterion	Drawing Specification
Chip	Chip in cross over area	1) Reject - if the chip causes crossover dot to be exposed 2) Chip on outside edge of the glass plate but is greater than 50% of glass thickness at crossover dot is reject able.	
Chip	Chip in contact pad area	Accept if:- a) X ≤ 2.0mm b) Y ≤ 0.5mm c) Z disregard	
	Chip in non-contact pad area	Accept if:- a) X ≤ 6.0mm b) Y ≤ 1.0mm c) Z disregard	

	Chip in perimeter seal area	Accept if:- a) Y ≤ 1/3 of perimeter seal width (W) b) X ≤ 3.0mm c) Z disregard d) X and Y not touch crossover dot	
Corner Chip	Corner chip within seal area	Accept if:- a) X ≤ 1/3 of perimeter seal width (W) b) Y ≤ 1/3 of perimeter seal width (W) c) Z disregard	
Defect Category	Defect Description	Criterion	Drawing Specification
	Corner chip not effecting contact pad / ITO	Accept if:- a) XY ≤ 4mm^2 AND b) Y ≤ D and X ≤ 2.0mm c) Z disregard	
	Corner chip effecting contact pad / ITO	A) Accept if:- a) XY ≤ 4mm^2 AND b) Y ≤ D and X ≤ 2.0mm B) Accept if:- a) X1 ≤ 2.0mm b) Y1 ≤ 0.5mm Z disregard	
Glass flare	A thin layer of glass flare at	Accept if:- a) Flare thickness ≤ ¼ W when W ≤	

	contact area	3mm b) Flare thickness ≤ 1mm when W > 3mm W: Contact ledge width	
Glass burr	A rough edge(s) left along the scribing edge (i.e. along the edges of display)	Reject – if the burr cause undersize or oversize of the LCD	Refer to LCD Physical Dimension Drawing
Rainbow	Colored ring in sharp blotches observed	Reject – if 3 or more colored rings in sharp blotches of color are observed. (Limit samples should be used when applicable)	
Defect Category	Defect Description	Criterion	Drawing Specification
Discoloration		Reject - if the discolorations enter the active viewing area of LCD. Color of the LCD shall follow product specification as specified in the manufacturing specification	
Air Void	LC does not fulfill the display	Reject	
Fill end contamination	Discoloration at end seal area	Reject if discoloration exceeded the baffle (for display with baffle) or viewing area (for display without baffle)	

10.2.3 POLARIZER DEFECT

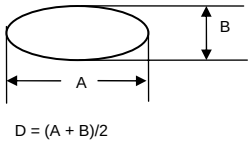
Defect Category	Defect Description	Criterion	Drawing Specification
Polarizer defect	Polarizer coverage	1- Polarizer should cover effective viewing area of display. 2- It is acceptable if perimeter seal bolder at all sides could be seen. 3- It is acceptable if polarizer attaching position meeting the tolerance mentioned in the drawing. 4- It is reject able if polarizer edge jagged and not even	Refer to LCD Physical Dimension Drawing
	Polarizer Peeling / delamination	1- Reject if any edge or corner of the polarizer is lifted up or not adheres to the glass	
	Polarizer Scratches	1- Any scratch should be acceptable if it is not visible from viewing distance at head of position 2-Polarizer scratch in viewing area is reject able if it is visible from the specified viewing distance 3-Defect, which is visible under surface glare, should be disregard	
	Polarizer damage	1-Stain mark or depression in front polarizer surface should be acceptable if it is not visible from viewing distance at head on position. 2-Defect, which is visible under surface glare, should be disregard	

Defect Category	Defect Description	Criterion	Drawing Specification
	Polarizer bubble / Foreign material	Zone /	Acceptable No.

Dimension	A		
D ≤ 0.15mm	NC	B	C
0.15 < D ≤ 0.30mm	3	NC	NC
0.30 < D ≤ 0.50mm	2	5	NC
0.50 < D ≤ 1.0mm	0	3	NC
NC: No count		1	NC

D: Mean Diameter of Defect

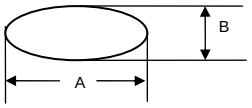
Accept - if air bubble at the seal area does not propagate into effective viewing area



D = (A + B)/2

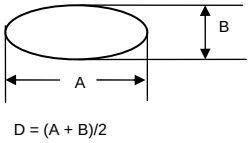
10.2.4 FUNCTIONAL DEFECT

<table>
<tr><th>Defect Category</th><th>Defect Description</th><th>Criterion</th><th>Drawing Specification</th></tr>
<tr><td>Missing common</td><td>Part of the pattern does not light up</td><td>Reject</td><td></td></tr>
<tr><td>Missing segment</td><td>One or few segment does not light up</td><td>Reject</td><td></td></tr>
<tr><td>Common-common short</td><td>Common and common connected</td><td>Reject</td><td></td></tr>
<tr><td>Segment-segment short</td><td>Segment and segment connected</td><td>Reject</td><td></td></tr>
<tr><td>Common – segment short</td><td>Common and segment connected</td><td>Reject</td><td></td></tr>
<tr><td>Wrong viewing angle</td><td>Wrong viewing angle</td><td>Reject if display viewing angle not conform to customer requirement</td><td></td></tr>
<tr><td>Metal residue</td><td>Extra spot lights up at the border of the segment.</td><td>Accept if ≤ 0.20mm (mean diameter)</td><td></td></tr>
<tr><td>Slow response</td><td>Response of the display on one side slower than the other side</td><td>Reject if it is visible at 30cm distance</td><td></td></tr>
<tr><td>Reverse twist/ tilt</td><td>Segment are darker or clearer than other area of the same segment</td><td>Reject</td><td></td></tr>
<tr><td>Misalignment</td><td>Segment fatter or smaller or extra segment</td><td>Reject if > 10% of designed segment width and visible at 30cm distance</td><td></td></tr>
<tr><td>Pin Hole</td><td>Pin hole / void at light up segment</td><td>
<table>
<tr><th rowspan="2">Zone / Dimension</th><th colspan="3">Acceptable No.</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>D ≤ 0.10mm</td><td>NC</td><td>NC</td><td>NC</td></tr>
<tr><td>0.10<D ≤ 0.20mm</td><td>3</td><td>3</td><td>NC</td></tr>
</table>
NC: No count

D: Mean Diameter of Defect</td><td> 

D = (A + B)/2</td></tr>
<tr><th>Defect Category</th><th>Defect Description</th><th>Criterion</th><th>Drawing Specification</th></tr>
<tr><td>Segment Smearing</td><td>Light up segment smear</td><td>Reject</td><td></td></tr>
<tr><td>Dim segment</td><td>Display shows poor contrast at pre set voltage</td><td>Reject</td><td></td></tr>
</table>

10.2.5 BLACK SPOT, WHITE SPOT AND FOEREIGN MATERIAL

Defect Category	Defect Description	Criterion				Drawing Specification
Black Spot, White Spot and Foreign Material	Black Spot, White Spot and Foreign Material	Zone / Dimension	Acceptable No.			
			A	B	C	
		D ≤ 0.10mm	NC	NC	NC	
		0.10<D ≤ 0.20mm	3	3	NC	
		0.20 < D ≤ 0.30mm	1	2	NC	
		D > 0.30 mm	0	0	NC	
		NC: No count D: Mean Diameter of Defect				

10.2.6 LINE SHAPE AND SCRATCHES

Defect Category	Defect Description	Criterion					Drawing Specification
Line shape and scratches	Line shape and scratches	Zone /Dimension		Acceptable No.			
		X	Y	A	B	C	
		-	<0.01mm	NC	NC	NC	
		< 2 mm	< 0.02mm	1	1	NC	
		<1 mm	< 0.0 2mm	1	2	NC	

Note: Total defects shall not exceed five

13. Precaution for using LCM

1. Liquid Crystal Display (LCD)

LCD is made up of glass, organic sealant, organic fluid and polymer based polarizers. The following precautions should be taken when handling.

b) Keep the temperature within the range of use and storage. Excessive temperature and humidity could cause polarization degredation, polarizer peel off or bubble.

c) Do not contact the exposed polarizer with anything harder than HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzin.

d) Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or colour fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.

e) Glass can be easily chipped or cracked from rough handling, especially at corners and edges.

f) Do not drive LCD with DC voltage.

2. Liquid Crystal Display Modules.

2.1 Mechanical Considerations

LCM are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modification. The following should be noted.

a) Do not tamper in any way with the tabs on the metal frame.

b) Do not modify the PCB by drilling extra holes, changing its outline, moving its component or modifying its pattern.

c) Do not touch the elastomer connector, especially insert a backlight panel (for example, EL)

d) When mounting a LCM make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.

a) Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.

2.2 Static Electricity

LCM contains CMOS LSI's and the same precaution for such devices should apply, namely

a) The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any parts of the human body.

b) The modules should be kept in antistatic bags or other containers to static for storage.

c) Only properly grounded soldering irons should be used.

d) If an electric screwdriver is used, it should be well grounded and shielded from commutator spark.

e) The normal static prevention measures should be observed for work clothes and working benches, the latter conductive (rubber) mat is recommended.

f) Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.

2.3 Soldering

a) Solder only to the I/O terminals.

b) Use only soldering irons with proper grounding and no leakage.

c) Soldering temperature: 280 °C

d) Soldering time: 3 to 4 sec

e) Use eutectic solder with resin flux fill.

f) If flux is used, the LCD surface should be covered to avoid flux spatters. Flux residue should be removed afterwards.

2.4 Operation

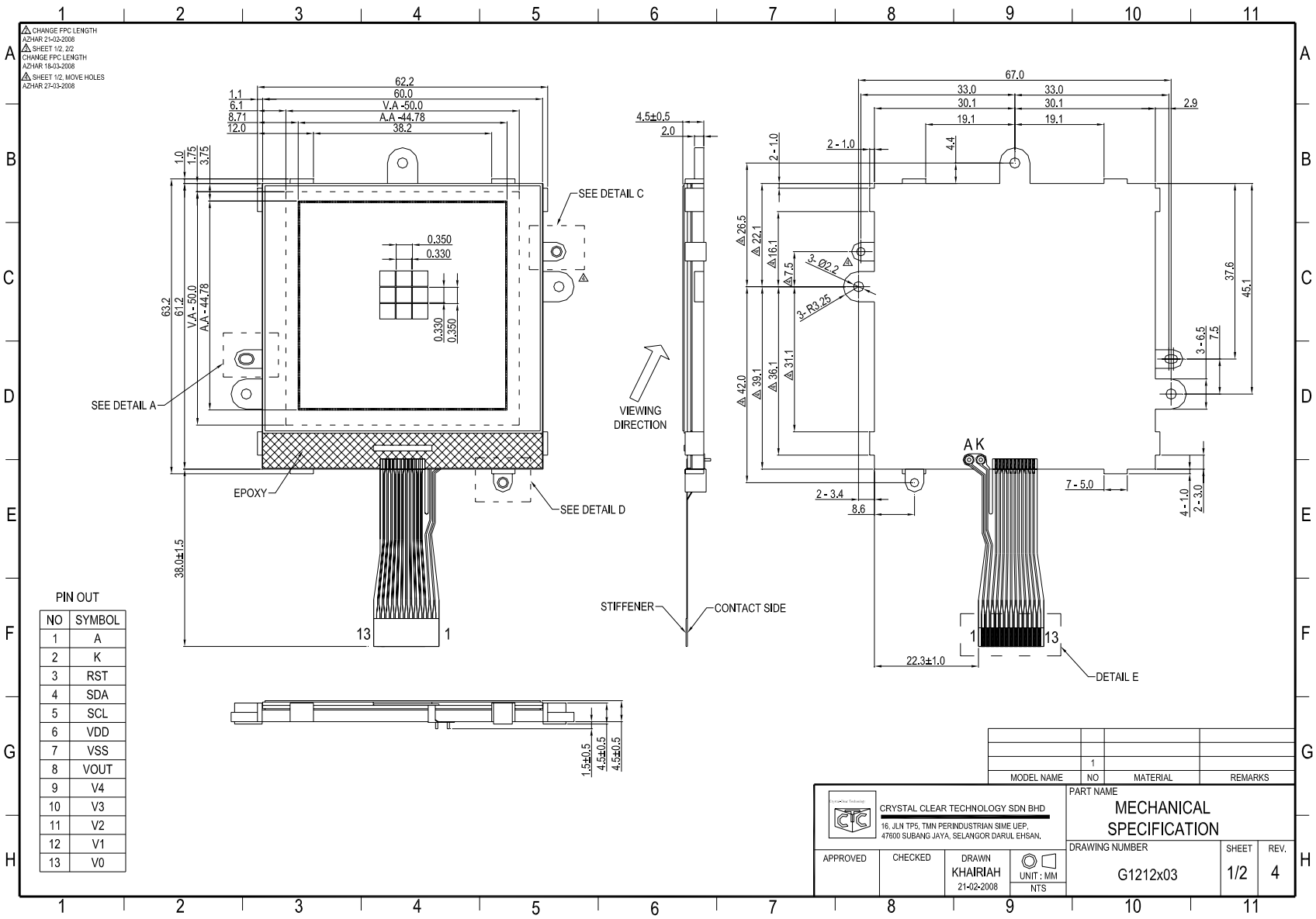
a) The contras can be adjusted by varying the LCD driving voltage V0
b) Driving voltage should be kept within specified range, excess voltage shortens display life.
c) Response time increases with decrease in temperature.
d) Display may turn black or dark blue at temperature above its operational range, this is (however not pressing on the viewing area) may cause the segments to appear "fractured".
e) Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured".

2.5 Storage

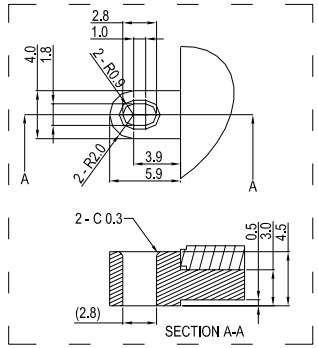
If any fluid leaks out of the damage glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all the time.

2.6 Limited Warranty

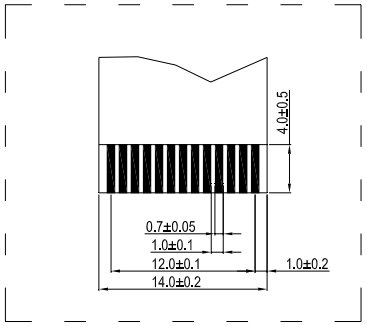
Unless otherwise agreed between Crystal Clear Technology and customer, Crystal Clear Technology will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with Crystal Clear Technology acceptance standards, for a period of one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of Crystal Clear Technology is limited to repair and/or replacement on the terms set forth above. Crystal Clear Technology will not responsible for any subsequent or consequential events.


CHANGE FPC LENGTH
AZHAR 21-02-2008
SHEET 1/2, 2/2
CHANGE FPC LENGTH
AZHAR 18-03-2008
SHEET 1/2, MOVE HOLES
AZHAR 27-03-2008
SEE DETAIL A
SEE DETAIL C
SEE DETAIL D
EPOXY
VIEWING DIRECTION
STIFFENER
CONTACT SIDE
DETAIL E
PIN OUT
NO SYMBOL
1 A
2 K
3 RST
4 SDA
5 SCL
6 VDD
7 VSS
8 VOUT
9 V4
10 V3
11 V2
12 V1
13 V0
MODEL NAME
NO
MATERIAL
REMARKS
CRYSTAL CLEAR TECHNOLOGY SDN BHD
16, JLN TP5, TMN PERINDUSTRIAN SIME UEP,
47600 SUBANG JAYA, SELANGOR DARUL EHSAN,
PART NAME
MECHANICAL SPECIFICATION
APPROVED
CHECKED
DRAWN
KHAIRIAH
21-02-2008
UNIT : MM
NTS
DRAWING NUMBER
G1212x03
SHEET
1/2
REV.
4

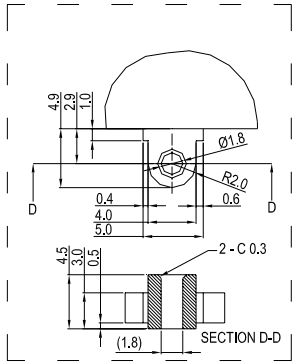
⚠ CHANGE FPC LENGTH
AZHAR 21-02-2008
⚠ SHEET 2/2
CHANGE FPC LENGTH
AZHAR 18-03-2008



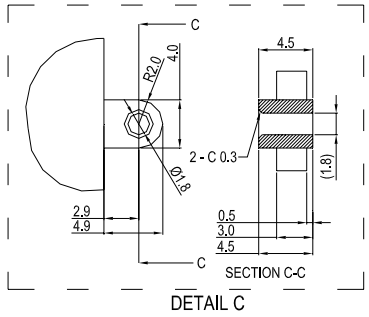
DETAIL A



DETAIL E



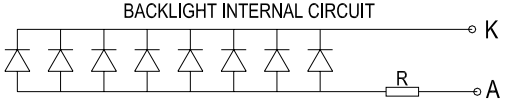
DETAIL D



DETAIL C

NOTE :-
1. DISPLAY :FSTN POSITIVE BLACK AND WHITE
2. VIEWING ANGLE: 6 O° CLOCK, DUTY CYCLE:1/128 DUTY BIAS:1/11
2. BACKLIGHT : YELLOW GREEN, 8 LEDS, Vf = 3.3V (typ), If = 80 mA
3. PIN OUT : REFER TABLE
4. DISPLAY : 128 X 128 DOTS
5. IC : SITRONIX ST7541
6. OPERATING TEMP:-5°C TO 50°C,STORAGE TEMP:-10°C TO 60°C
7. GENERAL TOLERANCE:±0.3
8. THIS MODULE IS RoHS COMPLIANT

BACKLIGHT INTERNAL CIRCUIT



MODEL NAME	NO	MATERIAL	REMARKS
	1		

CRYSTAL CLEAR TECHNOLOGY SDN BHD
16, JLN TP5, TMN PERINDUSTRIAN SIME UEP,
47600 SUBANG JAYA, SELANGOR DARUL EHSAN.

PART NAME: MECHANICAL SPECIFICATION

APPROVED	CHECKED	DRAWN	UNIT : MM	DRAWING NUMBER	SHEET	REV.
		KHAIRIAH 21-02-2008	NTS	G1212x03	2/2	4

Crystal Clear Technology
16 Jalan TP5—Taman Perindustrian Sime UEP
47600 Subang Jaya—Selangor DE
Malaysia